Virtex-4™ MB Development Board
User's Guide

Version 3.0
December 2005

Memec

Table of Contents

1 OVERVIEW 1

2 THE VIRTEX-4 MB SYSTEM BOARD 1

3 FUNCTIONAL DESCRIPTION 2

3.1 LVDS INTERFACE 3
3.1.1 SPI-4.2 Interface 4
3.1.2 SPI-4.2 Pin Assignments 4
3.1.3 LVDS Connector 6
3.2 DDR SDRAM 7
3.3 FLASH 8
3.4 CLOCK SOURCES 9
3.4.1 Programmable LVDS Clock Source 11
3.4.2 ICS8442 Programmable LVDS Clock Synthesizer 11
3.4.3 ICS8442 Clock Generation 13
3.4.4 ICS8442 Programming Modes 14
3.4.5 ICS8442 M and N Settings 14
3.5 10/100 ETHERNET PHY 18
3.6 LCD PANEL 20
3.7 USB 2.0 TO RS232 PORT 20
3.8 RS232 21
3.9 USER DIP AND PB SWITCHES 22
3.10 USER LEDS 23
3.11 VBAT JUMPER 23
3.12 CONFIGURATION AND DEBUG PORTS 23
3.12.1 JTAG Chain 23
3.12.2 System ACE Module Connector 24
3.12.3 Serial Data Flash 26
3.12.4 JTAG Port (PC4) 31
3.12.5 Configuration Modes 31
3.13 VOLTAGE REGULATORS 32
3.14 BANK I/O VOLTAGE 33
3.15 P240 EXPANSION MODULE SIGNAL ASSIGNMENTS 33

4 REVISIONS 36

APPENDIX A 37

Figures

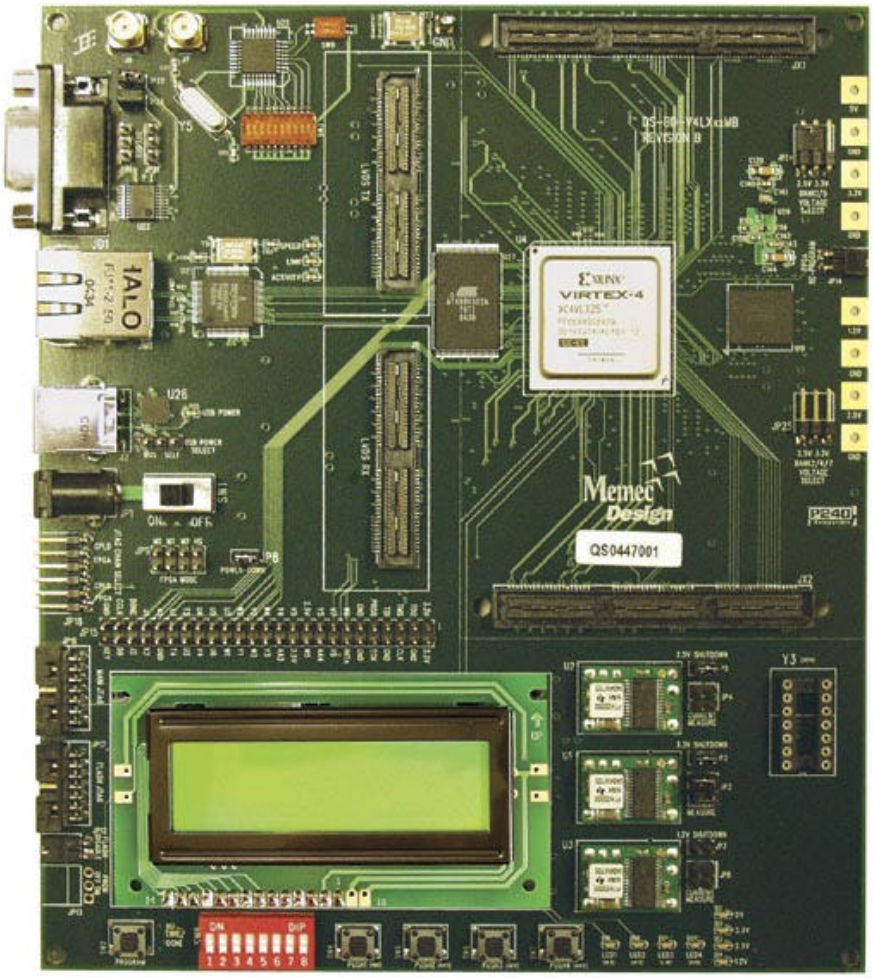
FIGURE 1 - VIRTEX-4 MB DEVELOPMENT PLATFORM BLOCK DIAGRAM 3
FIGURE 2- SPI-4.2 INTERFACE 4
FIGURE 3 – SAMTEC QSE TYPE CONNECTOR FOR THE SPI-4.2 INTERFACE 7
FIGURE 4 – DDR SDRAM INTERFACE 7
FIGURE 5 – FLASH INTERFACE 8
FIGURE 6 - CLOCK SOURCES ON THE VIRTEX-4 MB BOARD 10
FIGURE 7 – ICS8442 CLOCK SYNTHESIZER 12
FIGURE 8 – ICS8442 CLOCK SYNTHESIZER INTERFACE TO THE FPGA 15
FIGURE 9 – ICS8442 CLOCK SYNTHESIZER M AND N DIP SWITCHES 16
FIGURE 10 – M AND N DIP SWITCHES FOR THE SYNTHESIZERS 16
FIGURE 11 – 10/100 ETHERNET INTERFACE 19
FIGURE 12 – USB 2.0 TO RS232 SERIAL INTERFACE 21
FIGURE 13 - RS232 INTERFACE 22
FIGURE 14 – VITEX-4 MB DEVELOPMENT BOARD JTAG CHAIN 24
FIGURE 15 – SYSTEMACE MODULE 25
FIGURE 16 – VIRTEX-4 MB DEVELOPMENT BOARD CONFIGURATION INTERFACE 26
FIGURE 17 – VIRTEX-4 MB DEVELOPMENT BOARD JTAG CHAIN 28
FIGURE 18 – SERIAL FLASH CONFIGURATION INTERFACE 29
FIGURE 19 – PC4 JTAG PORT CONNECTOR 31
FIGURE 20 - VOLTAGE REGULATORS 32

1 Overview

The Memec Virtex-4™ MB Development Kit provides a complete development platform for designing and verifying applications based on the Xilinx Virtex-4 FPGA family. This kit enables designers to implement DSP and embedded processor based applications with extreme flexibility using IP cores and customized modules. The Virtex-4 FPGA along with Xilinx MicroBlaze soft processor core makes it possible to prototype processor based applications, enabling software design teams early access to a hardware platform prior to working with the final product/target board.

The Virtex-4 MB system board utilizes the Xilinx XC4VLX25/LX60/SX35-10FF668C FPGA. The board includes 64MB of DDR SDRAM, 4MB of Flash, 16-bit LVDS Transmit and Receive ports, programmable LVDS clock source, USB-RS232 Bridge, a 10/100 Ethernet PHY, 100 MHz clock source, RS-232 port, and additional user support circuitry to develop a complete system. The board also supports the Memec P240 expansion module standard, allowing application specific expansion modules to be easily added.

2 The Virtex-4 MB System Board



3 Functional Description

A high-level block diagram of the Virtex-4™ MB development platform is shown below followed by a brief description of each sub-section. A list of features for this board is shown below:

- Xilinx XC4VLX25/LX60/SX35-10FF668 FPGA
- 64MB of DDR SDRAM
- 4MB of Flash
- 16-Bit LVDS Transmit and Receive Interfaces
- 10/100 Ethernet PHY
- Programmable LVDS Clock Source (25-700 MHz)
- User LVDS Clock Outputs via Differential SMA Connectors
- On-board 100MHz LVTTL Oscillator
- On-board LVTTL Oscillator Socket (4/8-Pin Oscillators)
- P240 Connectors
- LCD Panel
- 32Mb Serial Flash for FPGA configuration
- PC4 JTAG Programming/Configuration Port
- SystemACE™ Module Connector
- RS232 Port
- Four User LEDs
- Four User Push Button Switches
- An 8-position DIP Switch
- USB-RS232 Bridge

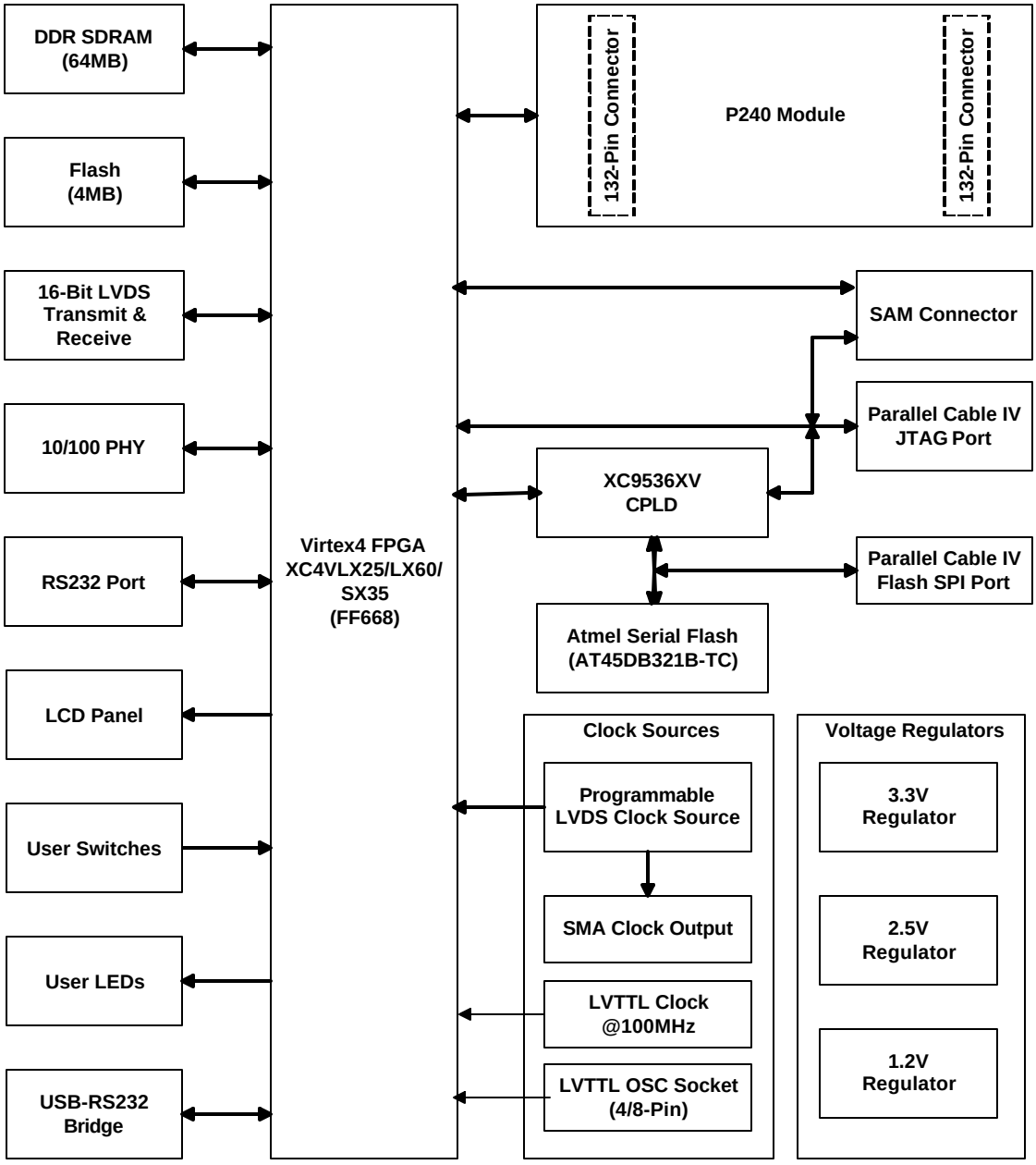


Figure 1 - Virtex-4 MB Development Platform Block Diagram

3.1 LVDS Interface

The Virtex-4 MB development board provides high-speed LVDS connectors supporting a SPI-4.2 interface. This interface consists of 36 LVDS signal pairs (72 FPGA signals) and 6 single-ended signals. In addition to the SPI-4.2 interface, the LVDS interface is designed to support XSBI 16-bit LVDS @644Mbps to support a 10GbE interface on the Virtex-4 MB development platform. The following sections provide a brief description of the LVDS interface on this development board.

3.1.1 SPI-4.2 Interface

The Virtex-4 MB development board provides a SPI-4.2 via a 16-bit parallel LVDS electrical interface. The following figure shows the SPI-4.2 interface on the board. The transmit and receive interface of the SPI-4.2 are implemented using LVDS signals while the status flow control signals are implemented using single-ended LVTTL signals.

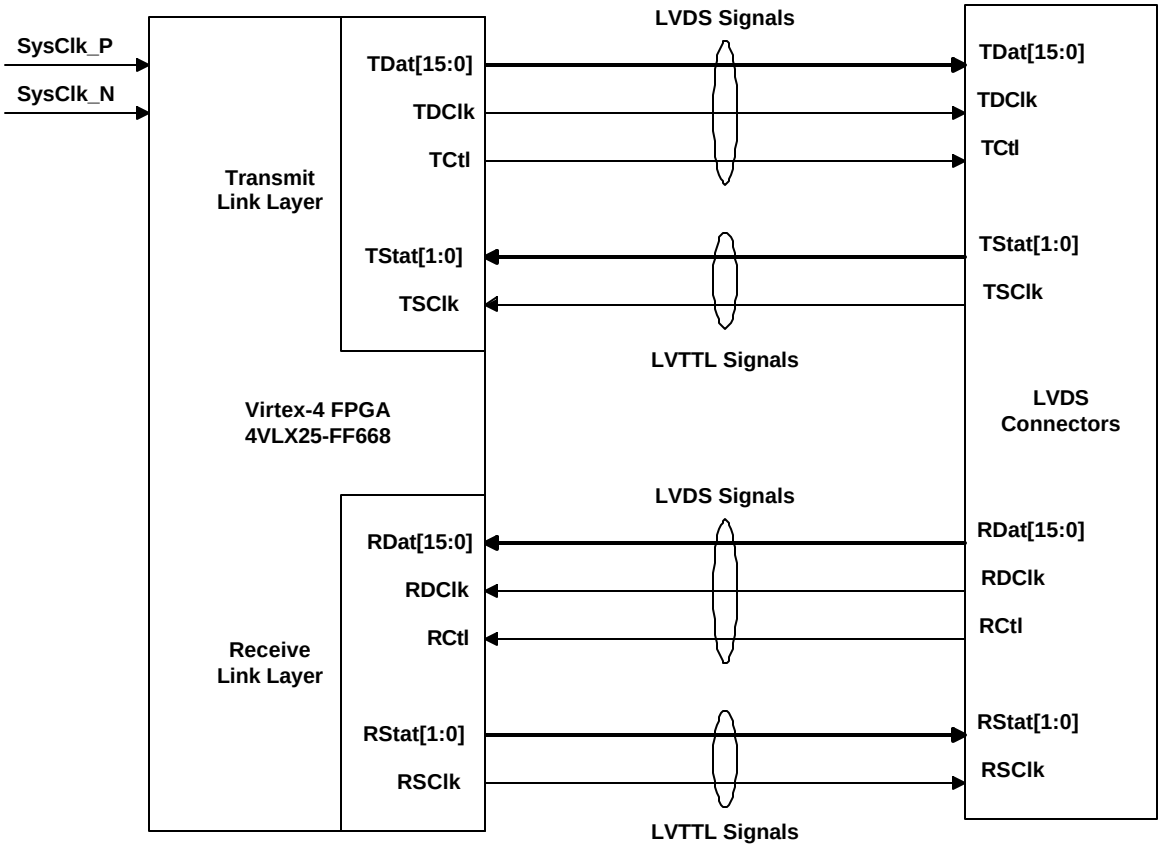


Figure 2- SPI-4.2 Interface

3.1.2 SPI-4.2 Pin Assignments

The following table shows the SPI-4.2 pin assignments for the 4VLX25/LX60/SX35 FPGA in the FF668-pin package. These pin assignments must be used in the board design in order to meet the SPI-4.2 interface core requirements.

Table 1– SPI-4.2 Transmit Pin Assignments

Virtex-4 Pin #	LVDS Signal Name	J4 Connector Pin # LVDS TX		LVDS Signal Name	Virtex-4 Pin #
	5.0V	1	2	**5.0V**	
	5.0V	3	4	**5.0V**	
	GND	5	6	**GND**	
	3.3V	7	8	**3.3V**	
	3.3V	9	10	**3.3V**	
	GND	11	12	**GND**	
	2.5V	13	14	**2.5V**	

	2.5V	15	16	**2.5V**	
	GND	17	18	**GND**	
R8	TSCLK	19	20	NC	
	NC	21	22	NC	
	GND	23	24	**GND**	
T8	TSTAT0	25	26	NC	
T7	TSTAT1	27	28	NC	
	GND	29	30	**GND**	
A7	TDat_N(15)	31	32	TDat_N(14)	D7
A8	TDat_P(15)	33	34	TDat_P(14)	D8
	GND	35	36	**GND**	
E10	TDat_N(13)	37	38	TDat_N(12)	A5
F10	TDat_P(13)	39	40	TDat_P(12)	A6
G8	TDat_N(11)	41	42	TDat_N(10)	C7
F8	TDat_P(11)	43	44	TDat_P(10)	B7
	GND	45	46	**GND**	
D5	TDat_N(9)	47	48	TDat_N(8)	B9
C5	TDat_P(9)	49	50	TDat_P(8)	A9
	GND	51	52	**GND**	
B3	TDat_N(7)	53	54	TDat_N(6)	D4
A3	TDat_P(7)	55	56	TDat_P(6)	C4
	GND	57	58	**GND**	
D6	TDat_N(5)	59	60	TDat_N(4)	E5
E7	TDat_P(5)	61	62	TDat_P(4)	E6
	GND	63	64	**GND**	
G7	TDat_N(3)	65	66	TDat_N(2)	C1
F7	TDat_P(3)	67	68	TDat_P(2)	C2
	GND	69	70	**GND**	
H7	TDat_N(1)	71	72	TDat_N(0)	E4
H8	TDat_P(1)	73	74	TDat_P(0)	D3
	GND	75	76	**GND**	
C8	TCtl_N	77	78	TDCLK_N	F9
D9	TCtl_P	79	80	TDCLK_P	E9
	GND	81	82	**GND**	
	GND	83	84	**GND**	
	GND	85	86	**GND**	
	GND	87	88	**GND**	

Table 2 – SPI-4.2 Receive Pin Assignments

Virtex-4 Pin #	LVDS Signal Name	J5 Connector Pin # LVDS RX		LVDS Signal Name	Virtex-4 Pin #
	5.0V	1	2	**5.0V**	
	5.0V	3	4	**5.0V**	
	GND	5	6	**GND**	
	3.3V	7	8	**3.3V**	
	3.3V	9	10	**3.3V**	
	GND	11	12	**GND**	
	2.5V	13	14	**2.5V**	
	2.5V	15	16	**2.5V**	
	GND	17	18	**GND**	
U5	RSCLK	19	20	NC	
	NC	21	22	NC	
	GND	23	24	**GND**	
J1	RSTAT0	25	26	NC	

J2	RSTAT1	27	28	NC	
	GND	29	30	**GND**	
AB4	RDat_N(15)	31	32	RDat_N(14)	AB2
AC4	RDat_P(15)	33	34	RDat_P(14)	AB3
	GND	35	36	**GND**	
AB5	RDat_N(13)	37	38	RDat_N(12)	AC1
AC5	RDat_P(13)	39	40	RDat_P(12)	AC2
AE3	RDat_N(11)	41	42	RDat_N(10)	AD1
AF3	TDat_P(11)	43	44	RDat_P(10)	AD2
	GND	45	46	**GND**	
AE4	RDat_N(9)	47	48	RDat_N(8)	AC3
AF4	RDat_P(9)	49	50	RDat_P(8)	AD3
	GND	51	52	**GND**	
AF5	RDat_N(7)	53	54	RDat_N(6)	Y7
AF6	RDat_P(7)	55	56	RDat_P(6)	AA7
	GND	57	58	**GND**	
Y9	RDat_N(5)	59	60	RDat_N(4)	AD4
AA9	RDat_P(5)	61	62	RDat_P(4)	AD5
	GND	63	64	**GND**	
Y1	RDat_N(3)	65	66	RDat_N(2)	V7
Y2	RDat_P(3)	67	68	RDat_P(2)	W7
	GND	69	70	**GND**	
Y8	RDat_N(1)	71	72	RDat_N(0)	AA10
AA8	RDat_P(1)	73	74	RDat_P(0)	Y10
	GND	75	76	**GND**	
AA1	RCtl_N	77	78	RDCLK_N	AF10
AB1	RCtl_P	79	80	RDCLK_P	AF11
	GND	81	82	**GND**	
	GND	83	84	**GND**	
	GND	85	86	**GND**	
	GND	87	88	**GND**	

3.1.3 LVDS Connector

The design of the SPI-4.2 interface requires use of a high-speed and high quality connector. The V4MB development board uses the SAMTEC QSE type connector for this interface. The **QSE-040-01-L-Dx-A** connector from SAMTEC provides up to 28 LVDS signal connections in addition to an adequate number of ground connections for improving the signal quality. Two of these connectors are used on the V4MB development board to implement the SPI-4.2 interface. In addition, a mating LVDS extension cable is available from Samtec (part number #**EQCD-040-06.00-TTR-TBL-1**). The following figure shows the QSE type connector from SAMTEC (the picture is obtained from the SAMTEC web site (http://www.samtec.com/).

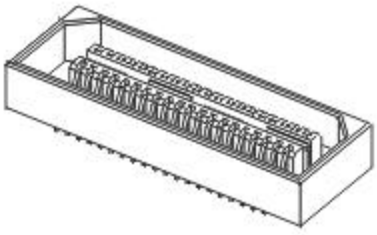


Figure 3 – SAMTEC QSE Type Connector for the SPI-4.2 Interface

3.2 DDR SDRAM

The Virtex-4™ MB development board provides 64MB of DDR SDRAM memory (x16). A high-level block diagram of the DDR SDRAM interface is shown below followed by a table describing the SDRAM memory interface signals.

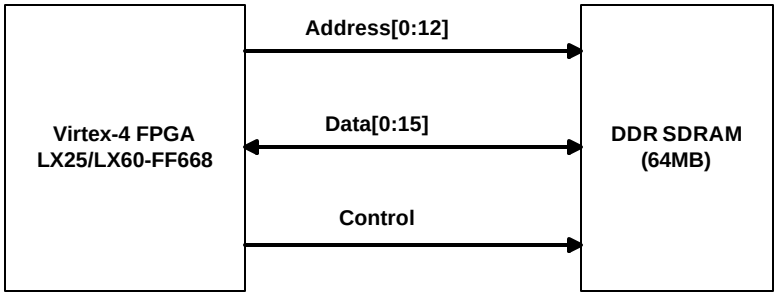


Figure 4 – DDR SDRAM Interface

Table 3 – DDR SDRAM Interface Pin Assignments

Signal Name	Description	FPGA Pin #
ddr_addr[0]	Address 0	N23
ddr_addr[1]	Address 1	K23
ddr_addr[2]	Address 2	N24
ddr_addr[3]	Address 3	J23
ddr_addr[4]	Address 4	V23
ddr_addr[5]	Address 5	P23
ddr_addr[6]	Address 6	U23
ddr_addr[7]	Address 7	P24
ddr_addr[8]	Address 8	T24
ddr_addr[9]	Address 9	R23
ddr_addr[10]	Address 10	K24
ddr_addr[11]	Address 11	T23
ddr_addr[12]	Address 12	R24
ddr_dq[0]	Data 0	K20
ddr_dq[1]	Data 1	J20
ddr_dq[2]	Data 2	L20

ddr_dq[3]	Data 3	J21
ddr_dq[4]	Data 4	M20
ddr_dq[5]	Data 5	K22
ddr_dq[6]	Data 6	N20
ddr_dq[7]	Data 7	J22
ddr_dq[8]	Data 8	T21
ddr_dq[9]	Data 9	P20
ddr_dq[10]	Data 10	T20
ddr_dq[11]	Data 11	T19
ddr_dq[12]	Data 12	U22
ddr_dq[13]	Data 13	P22
ddr_dq[14]	Data 14	U21
ddr_dq[15]	Data 15	U20
ddr_ba[0]	Bank Select 0	L23
ddr_ba[1]	Bank Select 1	M24
ddr_dm[0]	Write Mask0	M22
ddr_dm[1]	Write Mask1	N22
ddr_dqs[0]	Data Strobe0	M19
ddr_dqs[1]	Data Strobe1	N19
ddr_csn	Chip Select	L24
ddr_rasn	Row Address Strobe	M21
ddr_casn	Column Address Strobe	M23
ddr_wen	Write Enable	L21
ddr_clk	Clock	R20
ddr_clkn	Clock	R19
ddr_clke	Clock Enable	K21

3.3 Flash

The Virtex-4™ MB development board provides 4MB of flash memory (x16). A high-level block diagram of the flash interface is shown below followed by a table describing the flash memory interface signals.

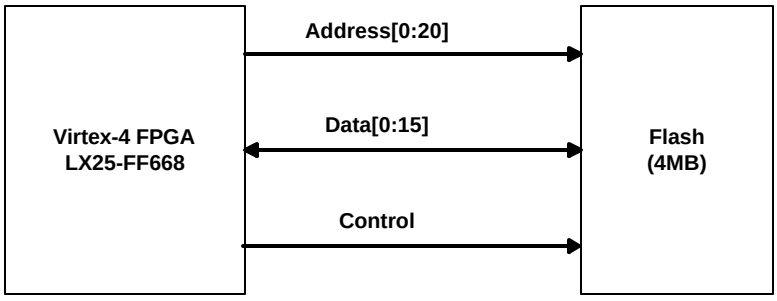


Figure 5 – Flash Interface

Table 4 – Flash Interface Pin Assignments

Signal Name	Description	FPGA Pin #
flash_addr[0]	Address 0	M2
flash_addr[1]	Address 1	T6
flash_addr[2]	Address 2	R5

flash_addr[3]	Address 3	P5
flash_addr[4]	Address 4	P6
flash_addr[5]	Address 5	P7
flash_addr[6]	Address 6	P8
flash_addr[7]	Address 7	N8
flash_addr[8]	Address 8	K6
flash_addr[9]	Address 9	J7
flash_addr[10]	Address 10	M7
flash_addr[11]	Address 11	M8
flash_addr[12]	Address 12	L8
flash_addr[13]	Address 13	K7
flash_addr[14]	Address 14	J4
flash_addr[15]	Address 15	J6
flash_addr[16]	Address 16	R3
flash_addr[17]	Address 17	N7
flash_addr[18]	Address 18	N5
flash_addr[19]	Address 19	L7
flash_addr[20]	Address 20	M6
flash_d[0]	Data 0	P2
flash_d[1]	Data 1	R2
flash_d[2]	Data 2	U1
flash_d[3]	Data 3	K3
flash_d[4]	Data 4	L3
flash_d[5]	Data 5	M4
flash_d[6]	Data 6	N4
flash_d[7]	Data 7	P3
flash_d[8]	Data 8	R1
flash_d[9]	Data 9	T1
flash_d[10]	Data 10	K4
flash_d[11]	Data 11	L4
flash_d[12]	Data 12	M3
flash_d[13]	Data 13	N3
flash_d[14]	Data 14	P4
flash_d[15]	Data 15	R4
flash_cen	Chip Select	M1
flash_oen	Output Enable	N2
flash_wen	Write Enable	J5
flash_rdy	Ready	M5
flash_reset	Reset	K5

3.4 Clock Sources

The Clock Generation section of the Virtex-4 MB board provides all the necessary clocks for a MicroBlaze processor, the I/O devices located on the board, as well as the DDR SDRAM memory. In general, the clock sources on the board are grouped into two categories; differential and single-ended clock sources. The differential clock sources are primarily used by the LVDS interface, while the single-ended clock sources are used by the processor section.

An on-board 100MHz oscillator provides the system clock input to the processor section. This 100Mhz clock will be used by the Virtex-4 Digital Clock Managers (DCMs) to generate various processor clocks. In addition to the above clock inputs, a socket is provided on the board that can

be used to provide single ended LVTTL clock input to the FPGA via an 8 or 4-pin oscillator. The following figure shows the clock resources on the Virtex-4 MB development board.

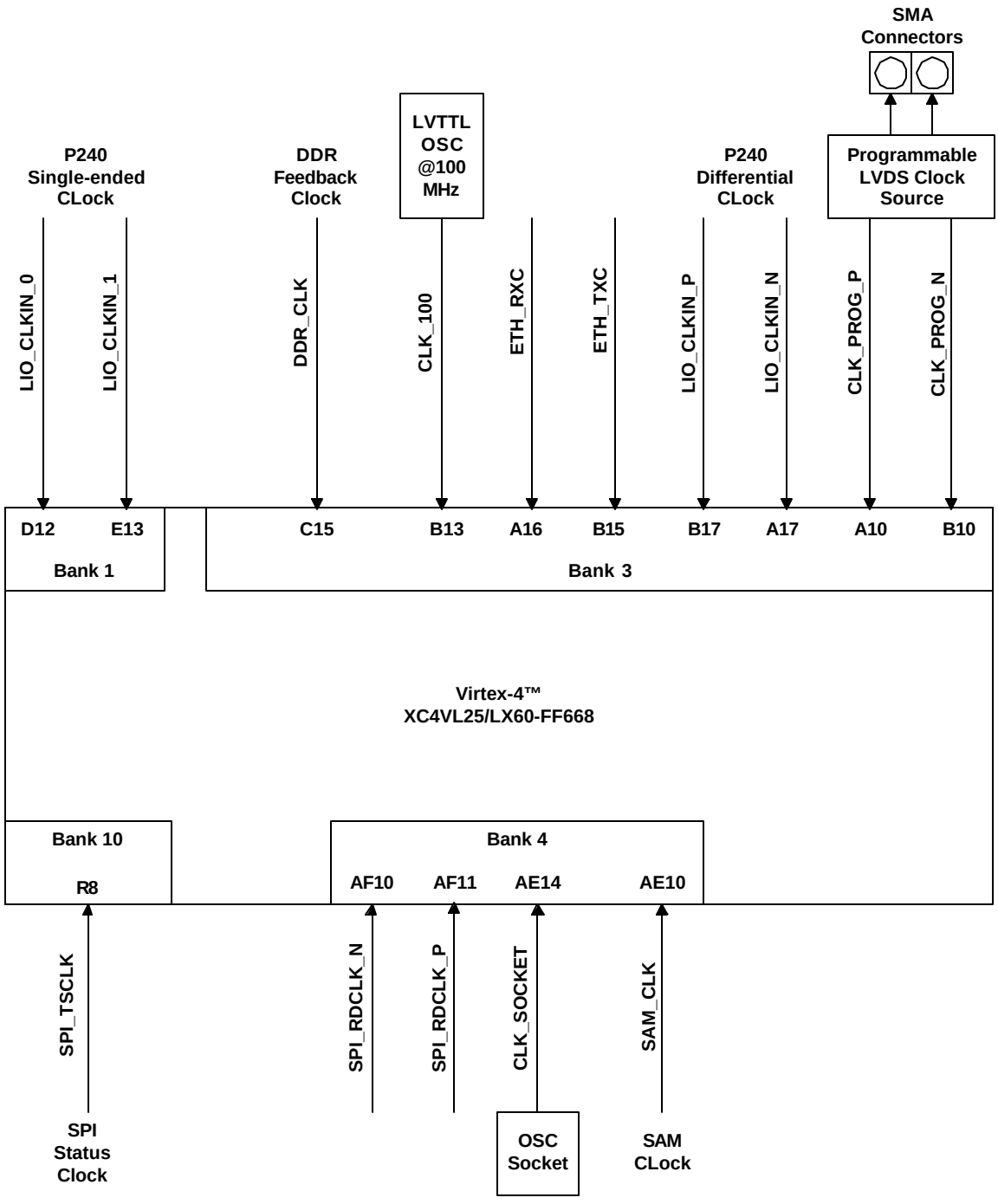


Figure 6 - Clock Sources on the Virtex-4 MB Board

The following table provides a brief description of each clock input to the Virtex-4 FPGA.

Table 5 - Clock Inputs

Signal Name	FPGA Pin #	Description
CLK_PROG_P, CLK_PROG_N	A10, B10	***Positive and Negative Differential System Clock Inputs*** – These clock inputs are connected to the output of an LVDS clock synthesizer. This programmable clock source can generate a clock frequency of 25 to 700MHz. Refer to the Programmable LVDS Clock Source section for more information.
LIO_CLKIN_P, LIO_CLKIN_N	B17, A17	***P240 Module Differential Clock Input*** – This clock input is connected to the P240 connector located on the Virtex-4 board.
LIO_CLKIN_0, LIO_CLKIN_1	D12, E13	***P240 Module Single-ended Clock Input*** s– These clock inputs are connected to the P240 connector located on the Virtex-4 board.
SPI_RDCLK_P, SPI_RDCLK _N	AF11, AF10	***Positive and Negative Differential SPI-4.2 Receive Clock Inputs*** – These clock inputs are connected to the LVDS receive connector on the Virtex-4 MB board. For the SPI-4.2 applications, these clock inputs are the SPI-4.2 receive clock outputs.
DDR_CLK	C15	***DDR Feedback Clock Input*** – This clock input is connected to the DDR clock.
CLK_100	B13	***System Clock*** – This clock input is connected to a 100MHz LVTTL oscillator.
CLK_SOCKET	AE14	***LVTTL Clock Input*** – LVTTL socket on the Virtex-4 board.
SPI_TSCLK	R8	***SPI-4.2 Transmit Status Clock Input*** – This clock input is connected to the SPI-4.2 transmit status clock output.
ETH_RXC	A16	***Ethernet Receive Clock Input*** – This clock input is connected to the Ethernet receive clock.
ETH_TXC	B15	***Ethernet Transmit Clock Input*** – This clock input is connected to the Ethernet transmit clock.
SAM_CLK	AE10	***SystemACE Module Clock Input*** – This clock input is connected to the SystemACE Module connector.

3.4.1 Programmable LVDS Clock Source

A programmable LVDS clock synthesizer is used on the Virtex-4 MB development board to generate a reference clock input to the LVDS interface. The use of this variable clock source, allows designers to prototype various interconnect technologies with different clock source requirements. The differential output port is also well suited for DSP applications when driving external DACs or ADCs.

3.4.2 ICS8442 Programmable LVDS Clock Synthesizer

The Virtex-4 MB development board design uses the ICS8442 LVDS clock synthesizer for generating various clock frequencies. A list of features included in the ICS8442 device is shown below.

- Output frequency range: 25MHz to 700MHz
- RMS period jitter: 2.7ps (typical)
- Cycle-to-cycle jitter: 27ps (typical)
- Output rise and fall time: 650ps (maximum)
- Output duty cycle: 48/52

The following figure shows a high-level block diagram of the ICS8442 programmable LVDS clock synthesizer.

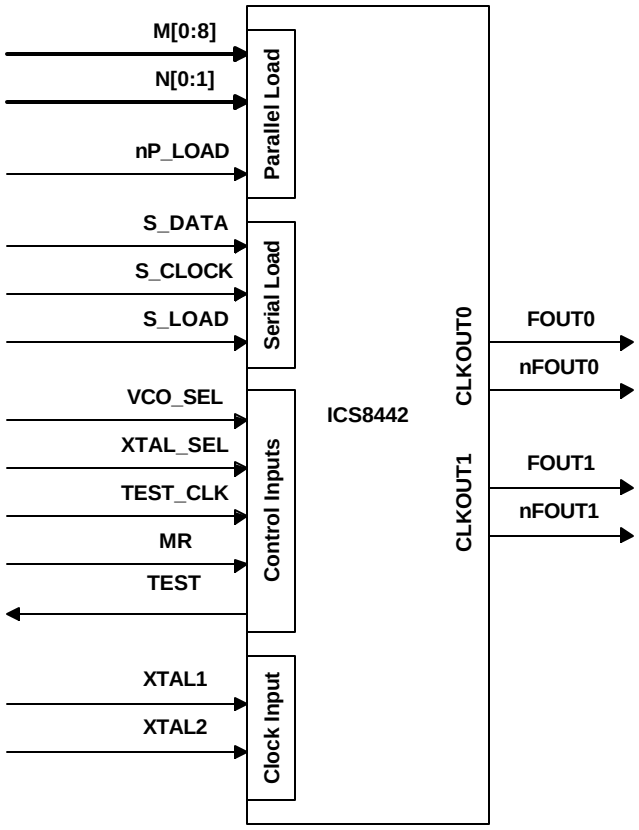


Figure 7 – ICS8442 Clock Synthesizer

Table 6 – ICS8442 Clock Synthesizer Pin Description

Signal Name	Direction	Pull up/Pull down	Description
M[0:4], M[6:8]	Input	Pull down	The M divider inputs, latched on the rising edge of the nP_LOAD signal.
M[5]	Input	Pull up	
N[0:1]	Input	Pull down	The N divider inputs, latched on the rising edge of the nP_LOAD signal.
TEST	Output		The TEST output is active during the serial mode of operations. Please refer to the datasheet for more information.
MR	Input	Pull down	Active high reset signal.
S_CLOCK	Input	Pull down	Serial interface clock input. Data is shifted into the device on the rising edge of this clock.
S_DATA	Input	Pull down	Serial interface data input.
S_LOAD	Input	Pull down	Serial interface load signal. The contents of the serial data shift register is loaded into the internal dividers on the rising edge of this signal.
TEST_CLK	Input	Pull down	Test clock input.
nP_LOAD	Input	Pull down	The rising edge of this signal is used to load the M and N divider inputs into the device.
XTAL1, XTAL2	Input		Crystal clock input/output

XTAL_SEL	Input	Pull up	This signal is used to select between the crystal and the TEST_CLK input to the device. When this high, crystal is selected.
VCO_SEL	Input	Pull up	This signal is used to place the internal PLL in the bypass mode. When this signal is set to low, the PLL is placed in the bypass mode. For normal operations, this signal must be set to high.
FOUT0, FOUT1	Output		Positive LVDS clock outputs
nFOUT0, nFOUT1	Output		Negative LVDS clock outputs

The Input Clock Select signals of the ICS8442 can be used to provide a reference clock input to the device other than the 25MHz crystal oscillator (for test purposes). The following table shows how these Input Clock Select signals are used to generate the output clock or to test the ICS8442 device. Please refer to the ICS8442 datasheet for more information on using the TEST_CLK clock input.

Table 7 – Input Clock Select Signal Description

VCO_SEL	XTAL_SEL	Reference Clock Input	FOUT[0:1]
0	0	TEST_CLK	TEST_CLK/N (the TEST_CLK must be between 10 and 25MHz). This mode can be used to test the ICS8442 device by routing the input clock to the outputs.
0	1	25MHz crystal	25MHz crystal/N (This mode can be used to test the ICS8442 device by routing the 25MHz crystal clock to the outputs).
1	0	TEST_CLK	ICS8442 PLL Output/N (Normal Operation)
1	1	25MHz crystal	ICS8442 PLL Output/N (Normal Operation)

3.4.3 ICS8442 Clock Generation

The ICS8442 output clocks are generated based on the following formula (assuming the crystal clock input is set to 25MHz):

$$FOUT[0:1] = 25 \times M/N$$

Where 8 < M < 28 and N can take a value of 1, 2, 4, or 8. The variable M is determined by setting the binary number M[0:8] while N is set according to the following table:

Table 8 – ICS8442 N Settings

N[1:0]	N	Output Clock Frequency Range (MHz)	
		Minimum	Maximum
00	1	200	700
01	2	100	350
10	4	50	175
11	8	25	87.5

For example, to generate a 62.5MHz clock, N[1:0] will be set to “10” (it can also be set to “11” since either one will be the correct frequency range for the 62.5MHz clock) and M will be set to “000001010” (decimal 10). So, from the above formula:

$$FOUT[0:1] = 25 \times 10/4 = 62.5Mhz$$

The following table shows how the M and N values can be set to generate a clock source for a few common applications. All the values for M and N are based on the 25MHz crystal clock input to the ICS8442 device. A complete list of frequencies generated by the ICS8442 (based on a 25MHz input clock) is provided in the following sections.

Table 9 – Examples of the ICS8442 M and N Settings

Interconnect Technology	FOUT0 and FOUT1 (MHz)	ICS8442 M and N Settings										
		M8	M7	M6	M5	M4	M3	M2	M1	M0	N1	N0
Gigabit Ethernet	62.5	0	0	0	0	0	1	0	1	0	1	0
Fiber Channel	53.125	0	0	0	0	1	0	0	0	1	1	1
	106.25	0	0	0	0	1	0	0	0	1	1	0
Infiniband	125	0	0	0	0	1	0	1	0	0	1	0
XAUI	156.25	0	0	0	0	1	1	0	0	1	1	0

3.4.4 ICS8442 Programming Modes

The ICS8442 provides two different methods of programming the M and N values into the device; a Parallel Mode and a Serial Mode. In parallel mode, M and N values are programmed into the device when the nP_LOAD signal pulses low. In the serial mode, the I2C pins (S_DATA and S_CLOCK) along with the S_LOAD signal are used to shift the M and N values into the device. Please refer to the ICS8442 datasheet for more information on programming modes of loading the M and N values into the device.

3.4.5 ICS8442 M and N Settings

The following figure shows how the ICS8442 programmable LVDS clock synthesizer is used on the Virtex-4 MB board. DIP Switches are provided on the board for manual setting of the M and N values.

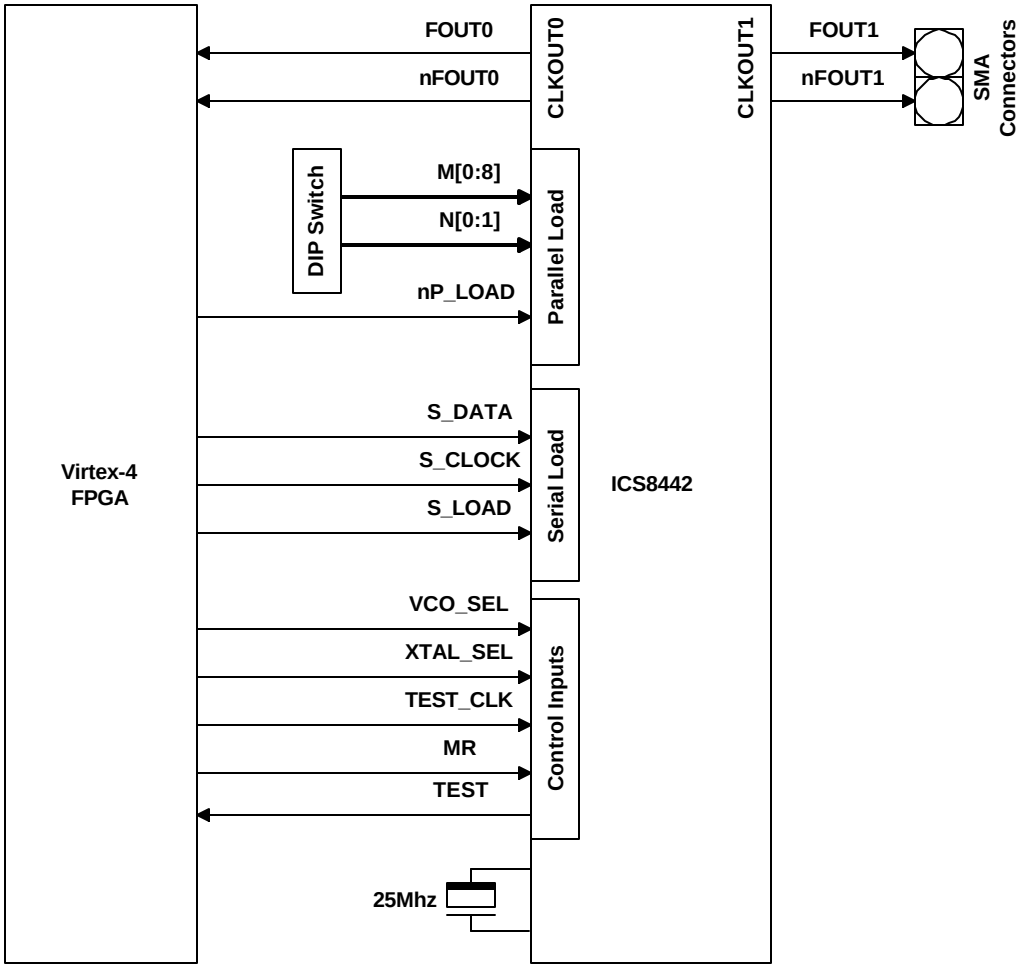


Figure 8 – ICS8442 Clock Synthesizer Interface to the FPGA

As shown in the above figure, the ICS8442 device outputs two identical LVDS clock sources. One of these clock sources can be used to provide the reference clock input to the LVDS interface on the Virtex-4 MB development board, while the other clock output can be used to trigger a scope during testing. The second output could also be used to provide a low jitter, LVDS clock source to a user board, such as the P240 module.

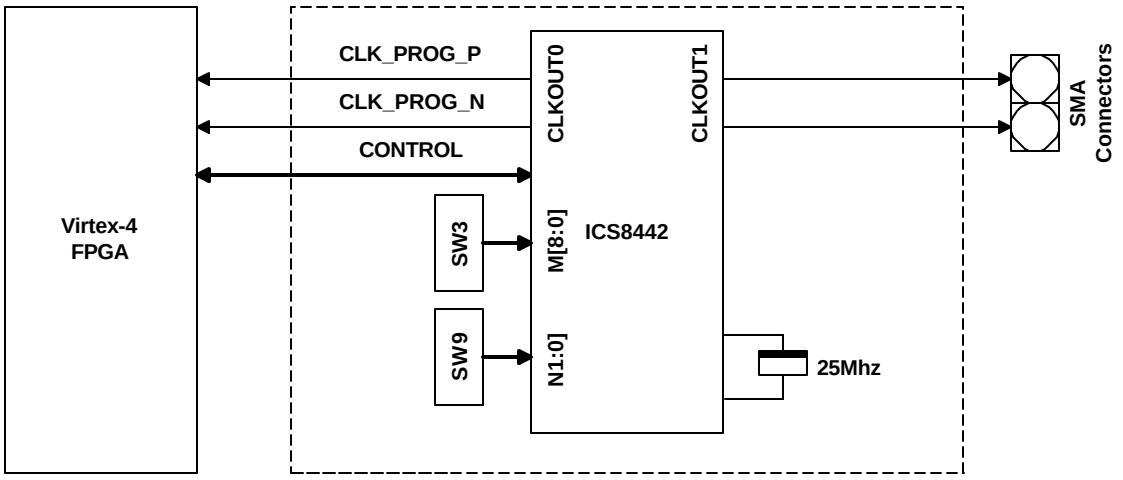


Figure 9 – ICS8442 Clock Synthesizer M and N DIP Switches

The following tables show the DIP Switch settings for M and N selections. Please refer to Table 6 for the information on pull-up and pull-down resistors provided internal to the ICS8442 device for the M and N input signals.

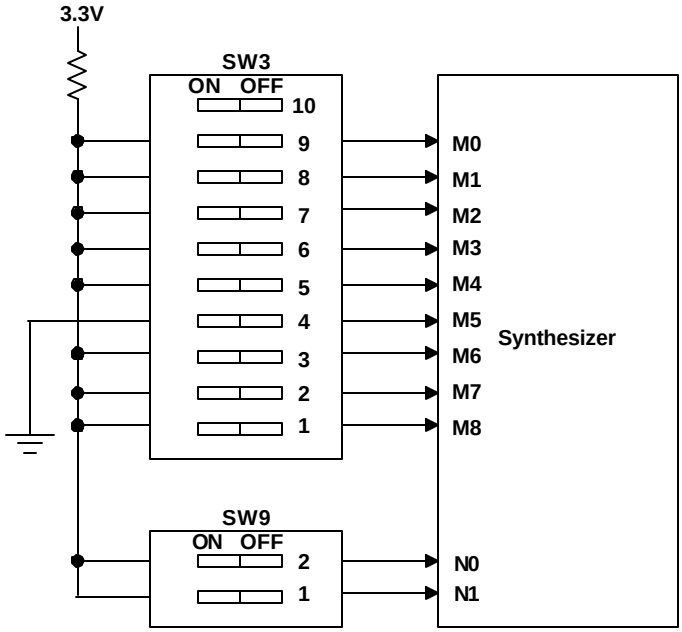


Figure 10 – M and N DIP Switches for the Synthesizers

Table 10 – DIP Switch Setting for M[8:0]

SW1, SW10, and SW2	M[8:0]	Switch Position	
		OFF	ON
DIP1	M8	0	1
DIP2	M7	0	1
DIP3	M6	0	1
DIP4	M5	1	0 Note (1)
DIP5	M4	0	1
DIP6	M3	0	1
DIP7	M2	0	1
DIP8	M1	0	1
DIP9	M0	0	1
DIP10	Unused	NA	NA

Note(1) – The polarity of M5 (DIP4) is the opposite of all other DIP switch positions.

Table 11 – DIP Switch Setting for N[1:0]

SW9, SW11, and SW13	N[1:0]	Switch Position	
		OFF	ON
DIP1	N1	0	1
DIP2	N0	0	1

The following table shows a complete list of frequencies generated by the ICS8442 device based on a 25MHz crystal reference clock input.

Table 12 – Synthesizer Clock Outputs for M and N Values

M[8:0]	N[1:0]	FOUT[1:0] (MHz)	M[8:0]	N[1:0]	FOUT[1:0] (MHz)
000001000	11	25 (Min)	000011000	10	150
000001001	11	28.125	000011001	10	156.25
000001010	11	31.25	000001101	01	162.5
000001011	11	34.375	000011010	10	162.5
000001100	11	37.5	000011011	10	168.75
000001101	11	40.625	000001110	01	175
000001110	11	43.75	000011100	10	175
000001111	11	46.875	000001111	01	187.5
000001000	10	50	000001000	00	200
000010000	11	50	000010000	01	200
000010001	11	53.125	000010001	01	212.5
000001001	10	56.25	000001001	00	225
000010010	11	56.25	000010010	01	225
000010011	11	59.375	000010011	01	237.5
000001010	10	62.5	000001010	00	250
000010100	11	62.5	000010100	01	250
000010101	11	65.625	000010101	01	262.5
000001011	10	68.75	000001011	00	275
000010110	11	68.75	000010110	01	275
000010111	11	71.875	000010111	01	287.5
000001100	10	75	000001100	00	300
000011000	11	75	000011000	01	300

000011001	11	78.125	000011001	01	312.5
000001101	10	81.25	000001101	00	325
000011010	11	81.25	000011010	01	325
000011011	11	84.375	000011011	01	337.5
000001110	10	87.5	000001110	00	350
000011100	11	87.5	000011100	01	350
000001111	10	93.75	000001111	00	375
000001000	01	100	000010000	00	400
000010000	10	100	000010001	00	425
000010001	10	106.25	000010010	00	450
000001001	01	112.5	000010011	00	475
000010010	10	112.5	000010100	00	500
000010011	10	118.75	000010101	00	525
000001010	01	125	000010110	00	550
000010100	10	125	000010111	00	575
000010101	10	131.25	000011000	00	600
000001011	01	137.5	000011001	00	625
000010110	10	137.5	000011010	00	650
000010111	10	143.75	000011011	00	675
000001100	01	150	000011100	00	700 (Max)

Table 13 – FPGA Pin Assignments for the Synthesizer Interface

Signal Name	Virtex-4 Pin #	Comments
SYNTH_PLOAD	V2	This input is used to load the M and N values into the synthesizer using the parallel mode configuration along with the DIP switch settings for M and N.
SYNTH_RESET	K1	This input signal resets the synthesizer.
SYNTH_SCLK	L1	This clock input is used to load the M and N values into the synthesizer using serial mode configuration.
SYNTH_SDATA	T4	Serial data input to the synthesizer for loading the M and N values.
SYNTH_SLOAD	T3	This input signal is used to load the M and N values into the synthesizer using the serial mode configuration.
SYNTH_TEST	U2	A test clock input can be provided to the synthesizer using this clock input.
SYNTH_VCOSEL	V1	This input signal can be used to bypass the PLL for test purposes.
SYNTH_XTALSEL	U3	This input signal is used to select between the test clock input and the on-board crystal as clock source to the synthesizer.
SYNTH_DOUT	K2	This output signal is used as the test clock output.

3.5 10/100 Ethernet PHY

The Virtex-4 MB development board provides a 10/100 Ethernet port for network connection. A high-level block diagram of the 10/100 Ethernet interface is shown in the following figure followed by FPGA pin assignments for this interface.

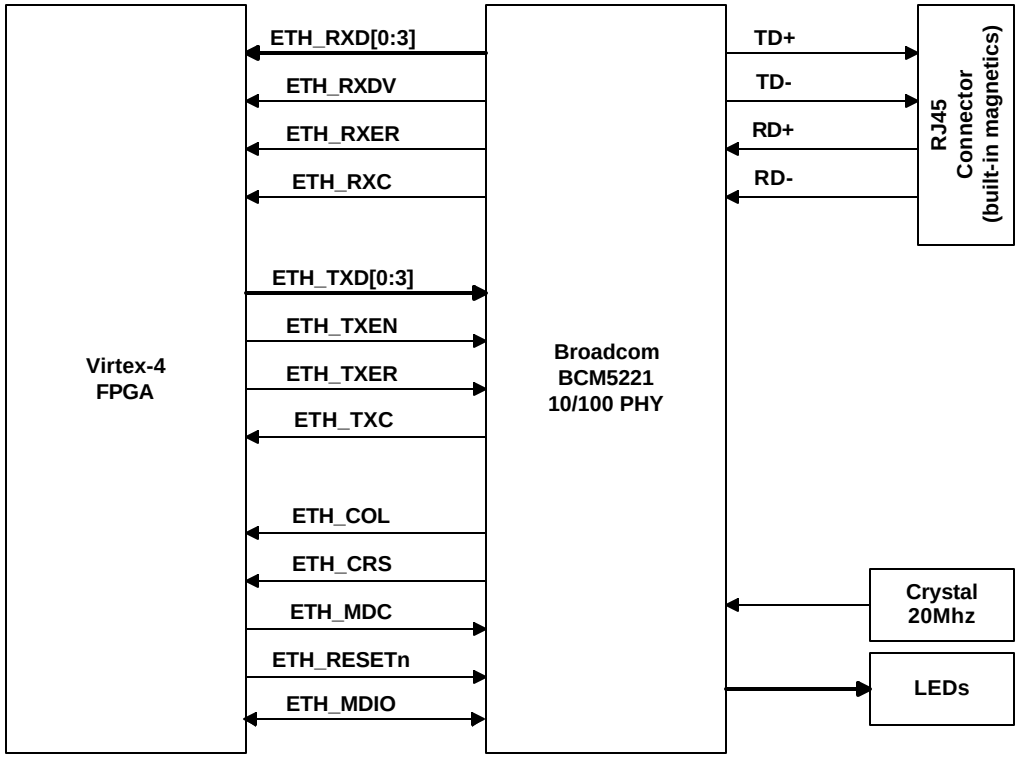


Figure 11 – 10/100 Ethernet Interface

The following table shows the FPGA pin assignments for the Ethernet interface.

Table 14 – Ethernet Pin Assignments

Signal Name	Virtex-4 Pin #
ETH_TXC	B15
ETH_RXC	A16
ETH_CRS	B14
ETH_RXDV	H1
ETH_RXD[0]	G4
ETH_RXD[1]	G3
ETH_RXD[2]	F3
ETH_RXD[3]	H4
ETH_COL	C14
ETH_RXER	H2
ETH_TXEN	G2
ETH_TXER	G1
ETH_TXD[0]	H5
ETH_TXD[1]	H6
ETH_TXD[2]	F1
ETH_TXD[3]	C12
ETH_MDC	F4
PHY_RESETn	E3
ETH_MDIO	H3

3.6 LCD Panel

The Virtex-4 MB development board provides an 8-bit interface to a 2x16 LCD panel (MYTECH MOC-16216B-B). The following table shows the LCD interface signals.

Table 15 – LCD Interface Signals

Signal Name	Description	Virtex-4 Pin #
D0	LCD Data Bit 0	K25
D1	LCD Data Bit 1	P19
D2	LCD Data Bit 2	AC10
D3	LCD Data Bit 4	AB10
D4	LCD Data Bit 4	AF12
D5	LCD Data Bit 5	AE12
D6	LCD Data Bit 6	AC17
D7	LCD Data Bit 7	AB17
EN	LCD Enable Signal	L19
RW	LCD Write Signal (this signal is connected to logic “0” on the Virtex-4 MB board, enabling write only cycles).	
RS	LCD Register Select Signal	N21

3.7 USB 2.0 to RS232 Port

The Virtex-4 MB development board implements a USB 2.0 port. This is accomplished using the Cygnal CP2101 USB-to-UART Bridge Controller. The FPGA interfaces to the CP2102 as a simple UART. The UART interface to the CP2102 can run at speeds ranging from 300 to 921,600 baud.

The CP2102 is a highly integrated USB-to-UART Bridge Controller, providing a simple solution for USB serial communications using a minimum of components and PCB space. The CP2102 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM, and asynchronous serial data bus (UART) with full modem control signals in a compact 5mm X 5mm MLP-28 package. No other external USB components are required.

The on-chip EEPROM may be used to customize the USB Vendor ID, Product ID, Product Description String, Power Descriptor, Device Release Number, and Device Serial Number as desired. The EEPROM is programmed on-board via the USB allowing the programming step to be easily integrated into the product manufacturing and testing process.

Royalty-free Virtual COM Port (VCP) device drivers provided by Cygnal allow the Virtex-4 MB development board to appear as a COM port to PC applications. The CP2102 UART interface implements all RS232 signals, including control and handshaking signals. These signals are interfaced to the Virtex-4 FPGA as follows:

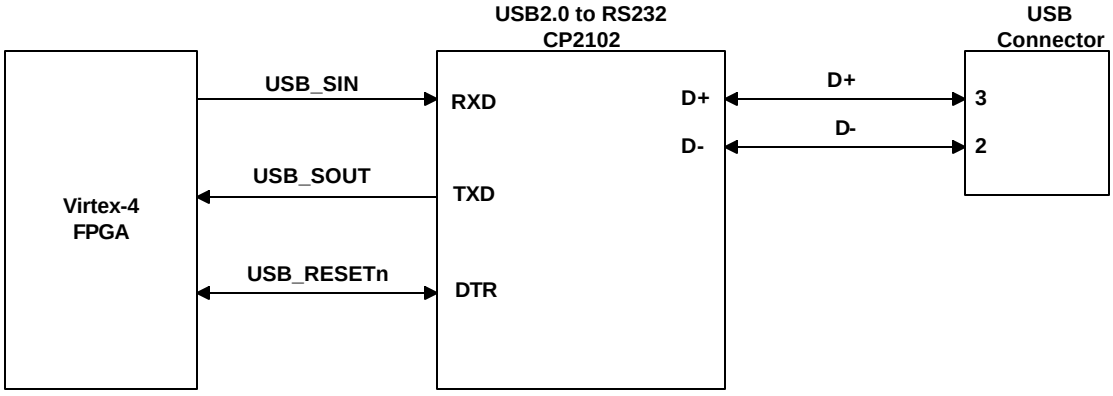


Figure 12 – USB 2.0 to RS232 Serial Interface

The following table shows the RS232 interface signal names and their Virtex-4 FPGA pin assignments.

Table 16- USB 2.0 to RS232 Port Signal Description

FPGA Signal Name	Virtex-4 Pin #	Description
RS232 Signals		
USB_SIN	R7	RS232 receive signal
USB_SOUT	L6	RS232 transmit signal
USB 2.0 Signals		
D+	NA	USB D+ signal
D-	NA	USB D- signal
Common Signal		
USB_RESETn	R6	CP2102 reset signal

To use the USB port, the CP2102 device drivers must be installed. These drivers are included on the Virtex-4 MB Development Kit CD and contained in the self-extracting file **CP2101.exe**. To install the CP2101/2 virtual COM port device drivers, refer to Appendix A.

3.8 RS232

The Virtex-4 MB development board provides an RS232 interface with RX and TX signals and jumpers for connecting the RTS and CTS signals. The following figure shows the RS232 interface to the Virtex-4 LX25/LX60/SX35 FPGA.

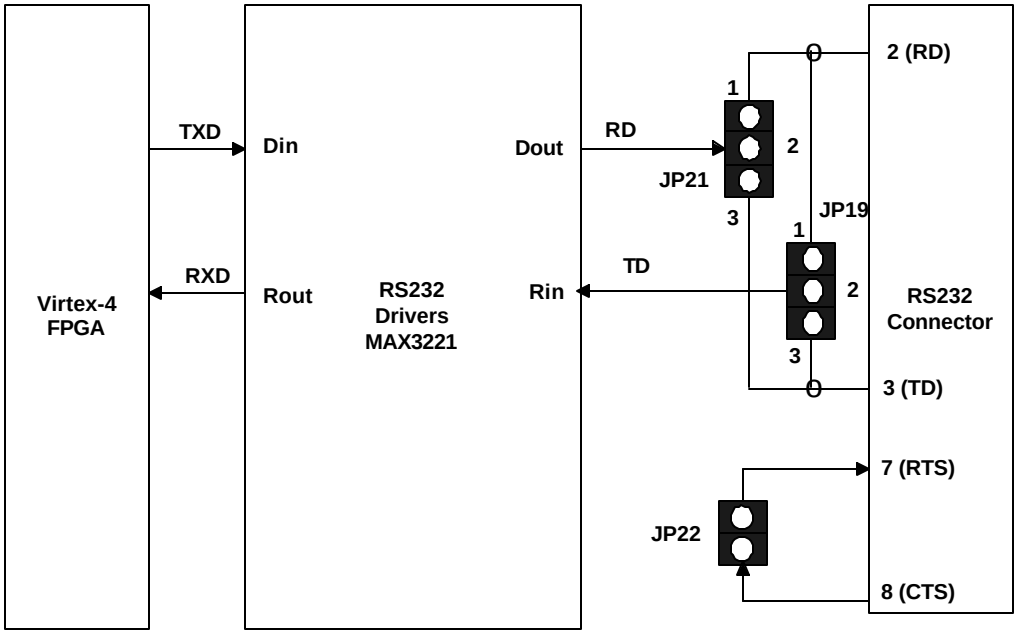


Figure 13 - RS232 Interface

Table 17 – RS232 Signals

Signal Name	Description	Virtex-4 Pin #
RS232_RXD	Received Data, RD	U4
RS232_TXD	Transmit Data, TD	V4

Table 18 - RS232 Jumper Settings

Mode of Operation	JP19	JP21
DCE	Install a jumper on pins 2-3	Install a jumper on pins 1-2
DTE	Install a jumper on pins 1-2	Install a jumper on pins 2-3

A Jumper must be installed on JP22, if RTS and CTS signal connections are needed.

3.9 User DIP and PB Switches

The Virtex-4 MB development board provides four user push button switches as described in the following table. An active low signal is generated when a given switch is pressed.

Table 19 – Push Button Switch Pin Assignments

Signal Name	Description	Virtex-4 Pin #
PUSH1	SW5	E2
PUSH2	SW6	E1
PUSH3	SW7	G10
PUSH4	SW8	G9

The Virtex-4 MB development board provides an 8-position DIP switch as described in the following table. An active low signal is generated when a given switch is ON.

Table 20 – DIP Switch Pin Assignments

Signal Name	Description	Virtex-4 Pin #
DIP1	User Switch Input 1	C10
DIP2	User Switch Input 2	D10
DIP3	User Switch Input 3	B6
DIP4	User Switch Input 4	C6
DIP5	User Switch Input 5	B4
DIP6	User Switch Input 6	A4
DIP7	User Switch Input 7	D2
DIP8	User Switch Input 8	D1

3.10 User LEDs

The Virtex-4 MB development board provides four user LEDs that can be turned "ON" by driving the LEDx signal to logic "0". The following table shows the user LEDs and their associated Virtex-4 FPGA pin assignments.

Table 21 – LED Pin Assignments

LED Designation	LED #	Virtex-4 Pin #
DS9	LED1	N25
DS10	LED2	V25
DS11	LED3	L26
DS12	LED4	K26

3.11 VBAT Jumper

A 3-pin jumper is used to provide user access to the VBAT input of the FPGA. If user is not sourcing the VBAT voltage, a jumper must be installed on pins 1-2 of the JP27 jumper. User can source voltage to the VBAT input via pins 2 and 3 of this jumper. The following table shows the pin assignments for the VBAT jumper.

Table 22 – VBAT Jumper (JP27)

Pin Number	Description
1	2.5V
2	VBAT
3	Ground

3.12 Configuration and Debug Ports

Various methods of configuration and debug support are provided on the Virtex-4 MB development board to assist designers during the testing and debugging of their applications. The following sections provide brief descriptions of each of these interfaces.

3.12.1 JTAG Chain

The following figure shows the JTAG chain on the Virtex-4 MB development board. The XC9536XV along with a serial flash is used to configure the FPGA. The serial flash programming procedure is explained in section 3.11.3.

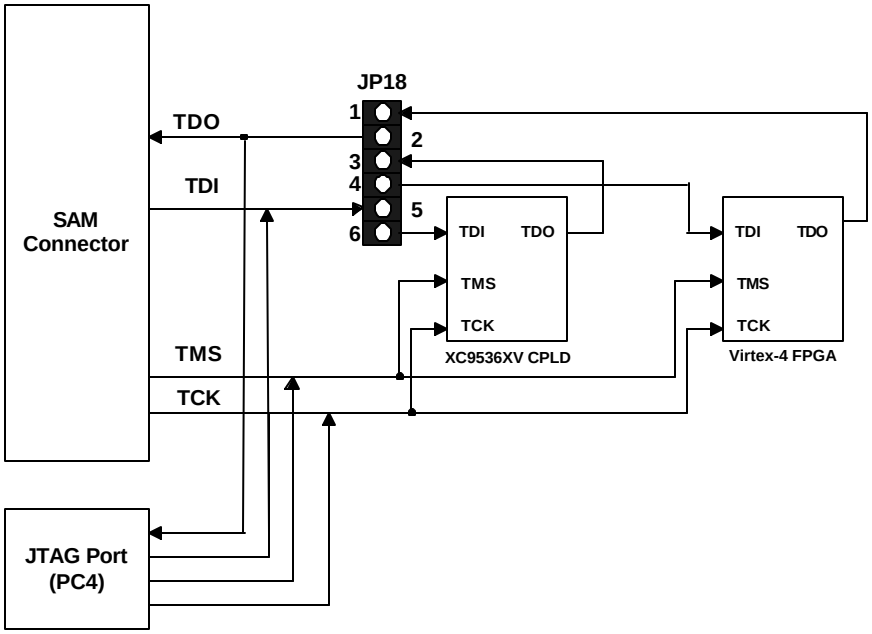


Figure 14 – Vitex-4 MB Development Board JTAG Chain

3.12.2 System ACE Module Connector

The Virtex-4 MB development board provides the SAM 50-pin connector on the board for using the Memec System ACE Module (SAM). The SAM can be used to configure the FPGA or to provide bulk flash memory to the MicroBlaze processor.

The Virtex-4 MB development board provides a System ACE interface that can be used to configure the Virtex-4 FPGA. The interface also gives software designers the ability to run real-time operating systems (RTOS) from removable CompactFlash cards. The Memec System ACE module (DS-KIT-SYSTEMACE) can be used to perform both of these functions. The figure below shows the System ACE module connected to the header on the Virtex-4 board.

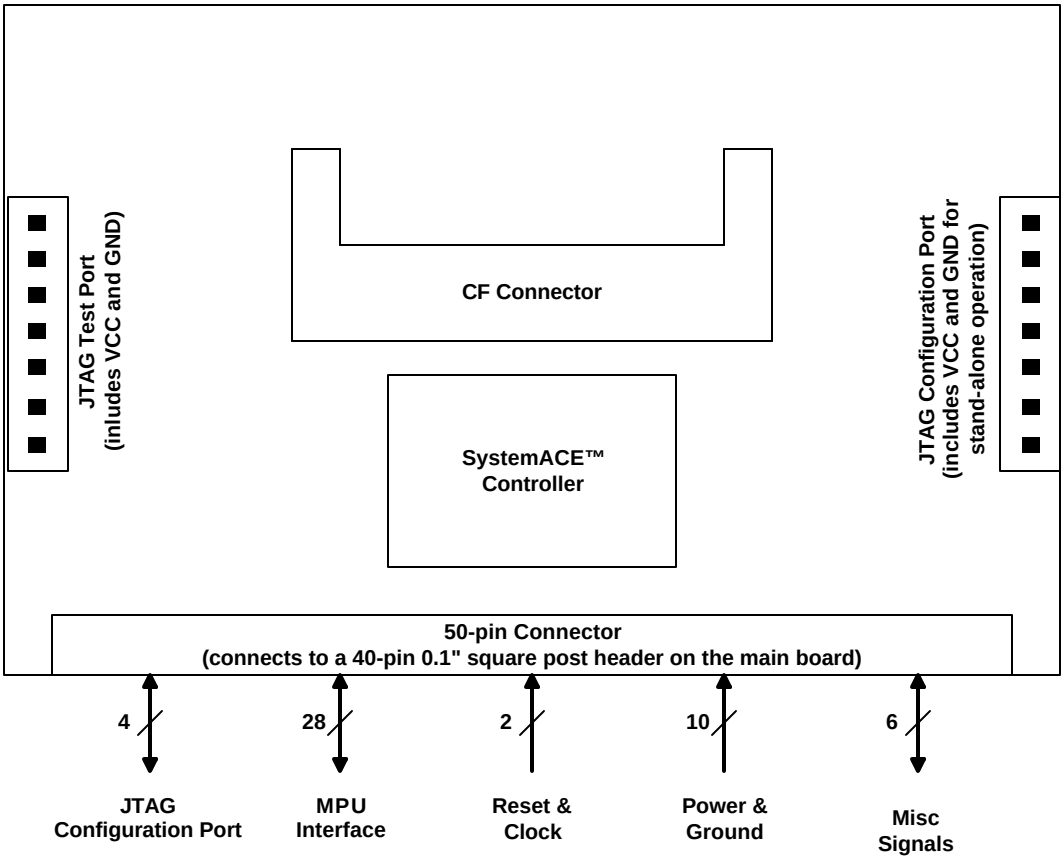


Figure 15 – SystemACE Module

3.12.2.1 System ACE Controller Signal Description

The following table shows the System ACE Module signal assignments to the FPGA I/O pins.

Table 23 - SAM Interface Signals

Virtex-4 Pin #	System ACE Signal Name	SAM Connector Pin # (JP16)		System ACE Signal Name	Virtex-4 Pin #
	3.3V	1	2	**3.3V**	
	TDO	3	4	**GND**	
	TMS	5	6	CLOCK	AE10
	TDI	7	8	**GND**	
	PROGRAMn	9	10	TCK	
	GND	11	12	**GND**	
AB7	OEn	13	14	INITn	
AB6	MPA0	15	16	WEn	V6
Y5	MPA2	17	18	MPA1	AC9
	2.5V	19	20	MPA3	AD8
V5	MPD00	21	22	**2.5V**	
AC7	MPD02	23	24	MPD01	AC8
AC6	MPD04	25	26	MPD03	AD6
AF9	MPD06	27	28	MPD05	AB9
AF8	MPD08	29	30	MPD07	AE9

AD10	MPD10	31	32	MPD09	AF7
AD11	MPD12	33	34	MPD11	AD12
AE6	MPD14	35	36	MPD13	AE13
W6	MPA4	37	38	MPD15	AA4
AA3	MPA6	39	40	MPA5	Y3
Y4	IRQ	41	42	**GND**	
W3	RESETn	43	44	CEn	W5
	DONE	45	46	BRDY	W4
	CCLK	47	48	BITSTREAM	
	GND	49	50	**NC**	

3.12.3 Serial Data Flash

This section describes the procedure for programming the Atmel serial data flash on the Memec Virtex-4 MB development board. This serial flash along with a CPLD is used to configure the Virtex-4 FPGA located on the development board on power up. The following figure shows a high-level block diagram of the serial flash interface to the Virtex-4 FPGA.

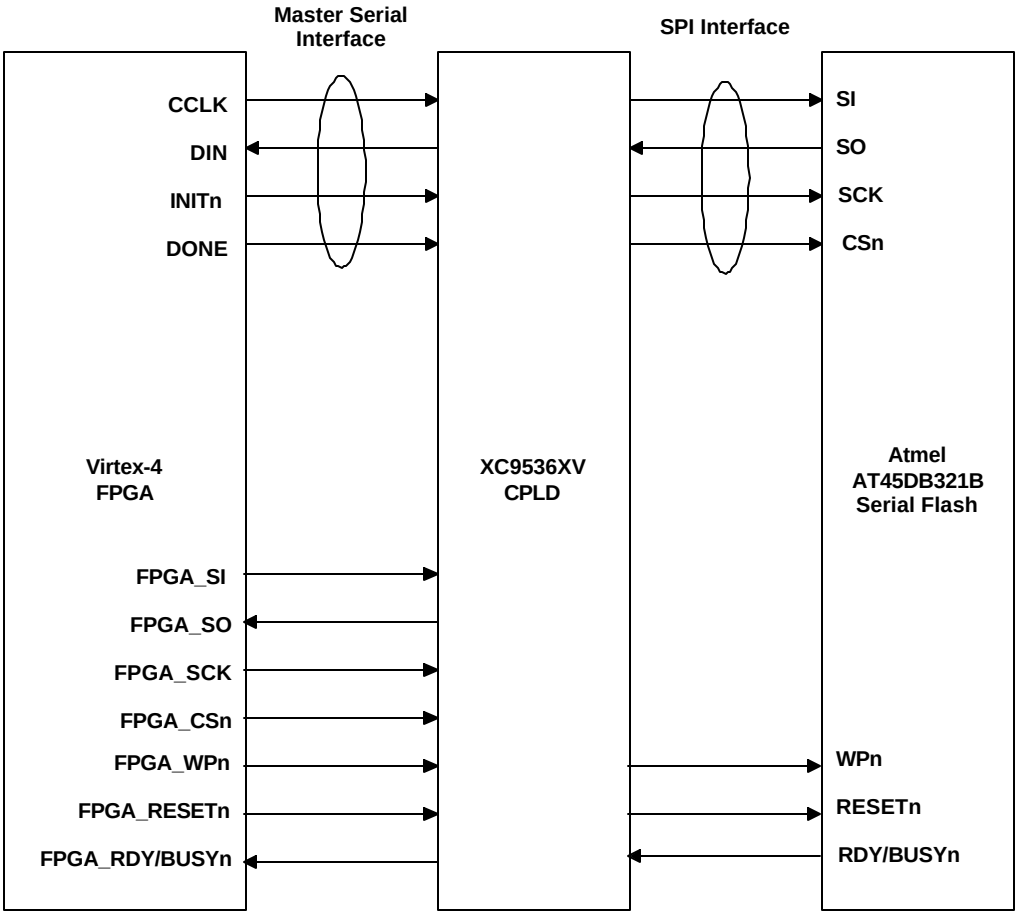


Figure 16 – Virtex-4 MB Development Board Configuration Interface

An interface is provided between the FPGA and the CPLD to allow access to the serial flash after the FPGA has been configured. This interface uses FPGA I/O pins to interface to the serial flash via the SPI port. The Virtex-4 FPGA uses 8Mb/18.3Mb/14.5Mb (LX25/LX60/SX35) of the serial flash memory for configuration and this interface allows the rest of the flash to be used for general-purpose application after the FPGA has been configured. The following table shows the signals used to implement the interface between the FPGA and the CPLD after the FPGA has been configured.

Table 24 – FPGA SPI Interface Pin Assignments

Signal Name	Description	Virtex-4 Pin #
FPGA_SI	Serial Flash SPI port data input signal	R26
FPGA_SO	Serial Flash SPI port data output signal	T26
FPGA_SCK	Serial Flash SPI port clock input signal	P25
FPGA_CSn	Serial Flash SPI port chip select input signal	U26
FPGA_WPn	Serial Flash SPI port write protect input signal	U25
FPGA_RESETn	Serial Flash SPI port reset input signal	M25
FPGA_RDY/BUSYn	Serial Flash SPI port ready output signal	V26

The primary function of the CPLD is to translate the Master Serial interface to the SPI interface of the serial flash. The XC9536XV CPLD uses the FPGA CCLK clock along with the INITn and DONE signals to drive the SPI SI, SCK and CSn signals. The SO output of the serial flash is used by the CPLD to drive the DIN signal of the FPGA. For more information on detail of the CPLD design, please refer to the Xilinx XAPP800.

3.12.3.1 JTAG Chain on the Virtex-4 MB Development Board

The following figure shows the JTAG chain on the Virtex-4 MB development board. As mentioned in the above section, the CPLD is used for interfacing to the configuration flash and does not provide any user logic. Hence, this CPLD is programmed by Memec prior to shipping the board. The programming file for the CPLD is provided in case re-programming of the CPLD becomes necessary. **The CPLD must be programmed prior to performing any operations on the serial flash such as erasing, programming, reading or verifying**.

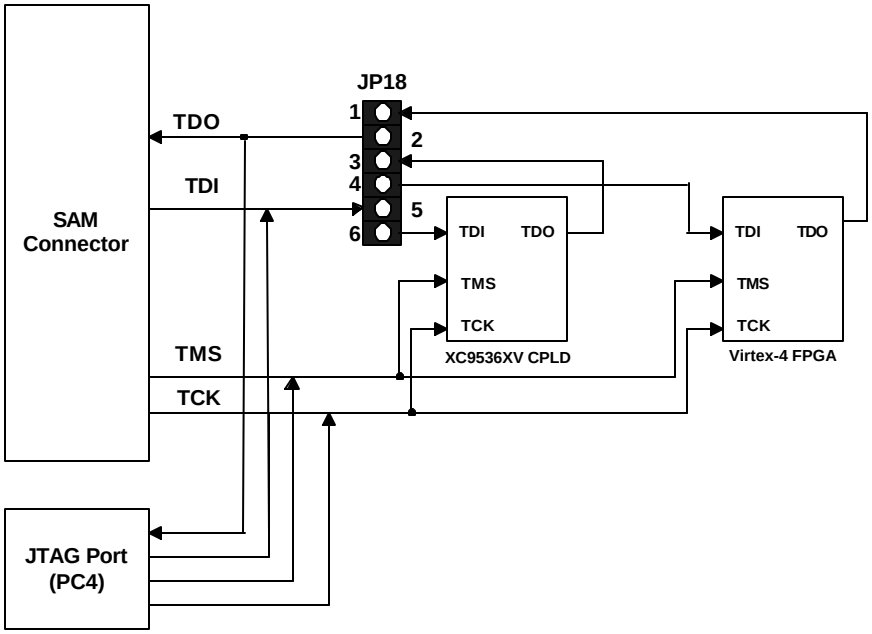


Figure 17 – Virtex-4 MB Development Board JTAG Chain

The following table shows jumper settings for the JTAG chain on the Virtex-4 MB development board. Since CPLD is already programmed by Memec prior to shipment, the board is shipped with jumpers installed on pins 1-2 and 4-5 (FPGA only, in the JTAG chain).

Table 25 – JTAG Chain Jumper Settings

Devices in the JTAG Chain	JP18 Jumpers Installed
CPLD and FPGA	Pins 1-2, 3-4 and 5-6
CPLD	Pins 2-3 and 5-6
FPGA	Pins 1-2 and 4-5

3.12.3.2 Configuration Flash on the Virtex-4 MB Development Board

The following figure shows the detail interface between the FPGA and the serial flash. A PC4 cable is used to program the serial flash with the FPGA bitstream. Once the flash is programmed, the CPLD will read the data from the flash and configure the FPGA over the Master Serial interface.

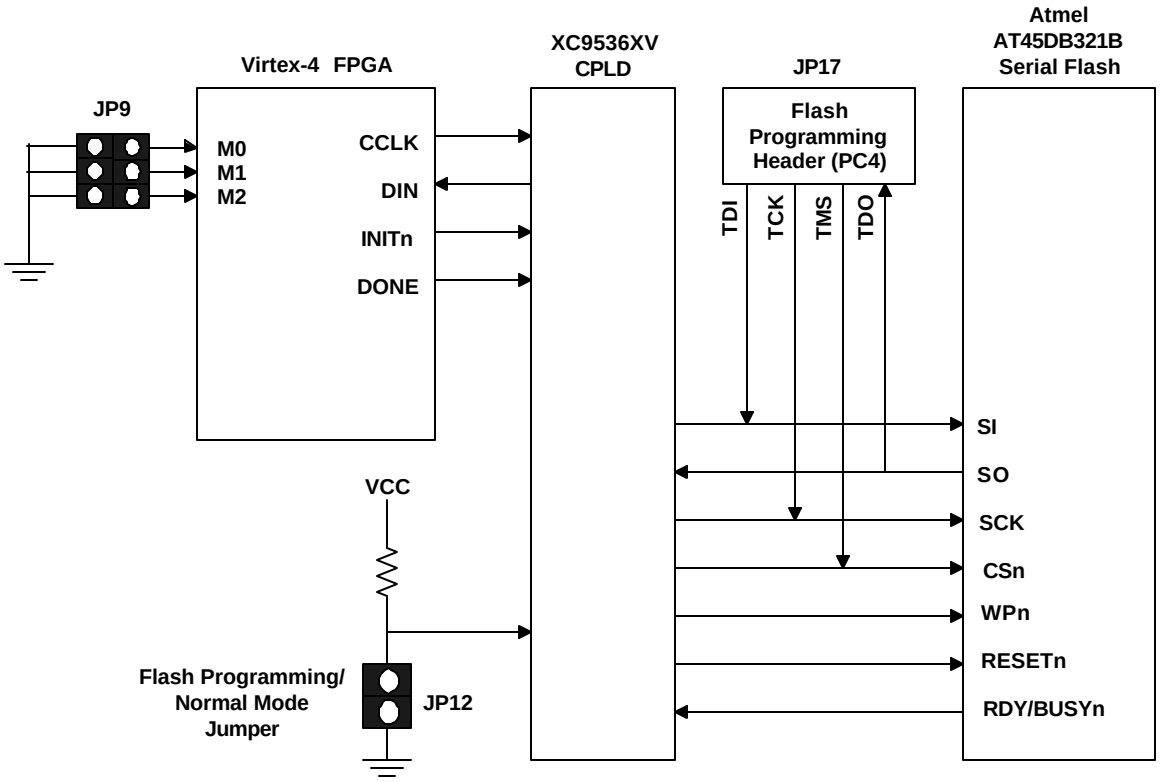


Figure 18 – Serial Flash Configuration Interface

3.12.3.3 Procedure for Programming the Serial Flash

1. The Memec Virtex-4 MB development board is shipped with a self-extracting zip file called **Serial_Flash_Programming**. Double-click on this self-extracting zip file to unzip it. After unzipping this file, a folder called **C:\Flash_Utilities** is created.

2. In order to program the flash, flash programming utilities included in the **xapp800** must be downloaded from the following web site:
   http://www.xilinx.com/products/xaw/coolvhdlq.htm

3. Click on the above link to download the **xapp800** zip file and unzip it to a temporary folder on your hard drive. You need to register prior to downloading the xapp800 zip file.

4. Copy **xmcsutil.exe** and **xspi_at.exe** files from this temporary folder to the C:\Flash_Utilities folder. The following table shows the contents of the C:\Flash_Utilities folder after copying these two executable files.

Table 26 – Files in the Flash_Utilities Folder

File Name	Description

xmcsutil.exe	A utility that is used to reverse the bytes in an MCS file. This is needed by the xspi_at utility.
xspi_at.exe	This utility is used to erase, program and verify the Atmel serial flash on the Virtex-4 MB development board.
prog_flash.bat	This batch file calls the xmcsutil and xspi_at utilities to erase, program and verify the Atmel serial flash on the Virtex-4 MB development board.
spi_cpld.jed	Programming file for the XC9536XV CPLD

5. Generate a bit file for the FPGA

6. Use iMPACT to generate an MCS file for the bit file generated in the previous step. When generating the MCS file, select a single platform flash device that will hold the entire design configuration bits. The following table shows the platform flash devices that must be used when generating the MCS file in iMPACT for the Virtex-4 MB board:

Table 27 – Platform Flash Selection

FPGA	Platform Flash Used
LX25	XCF08P, XCF16P or XCF32P
LX60	XCF32P
Sx35	XCF16P or XCF32P

7. Un-install JP9 jumpers.

8. Make sure JP12 jumper is un-installed. When JP12 jumper is un-installed, the CPLD outputs are placed in the tri-state mode allowing the Flash Programming Header to drive the serial flash SPI bus.

9. Connect a PC4 cable to the Flash Programming Header (JP17) and power up the Virtex-4 MB development board.

10. Copy the MCS file to the **C:\Flash_Utilities** folder

11. Open a DOS window in the **C:\Flash_Utilities** folder and enter the following command to program the serial flash:

    C:\ Flash_Utilities > prog_flash design_name.mcs flash_part_number

    Where: **design_name.mcs -> The mcs file generated using the bit file**

    flash_part_number -> Either AT45DB321B or AT45DB321C (V4MB board is populated with one or the other device).

    The prog_flash batch file will erase the flash, program and verify it.

12. Once the flash programming is completed, open the **verify_result.txt** file in the C:\Flash_Utilities folder. If the flash programming was successful, you should see the following line in the verify_result.txt file:

    --> Total byte mismatches [0]

    If there is anything other than this line in the verify_result.txt file, the flash programming was NOT successful. Check the following jumper settings:

    a. Make sure JP9 jumpers are un-installed.
    b. Make sure JP12 jumper is un-installed.

    After checking these jumper settings go back to the step 11 and re-program the flash.

13. Upon completion of the serial flash programming, power down the board and **remove the PC4 cable from the Flash Programming header**.

14. Set the mode jumpers to Master Serial (install all mode jumpers on JP9)

15. Install a jumper on JP12.

16. Power up the board and FPGA will configure.

3.12.4 JTAG Port (PC4)

The Virtex-4 MB development board provides a JTAG port (PC4 type) connector for configuration of the FPGA. The following figure shows the pin assignments for the PC4 header on this development board.

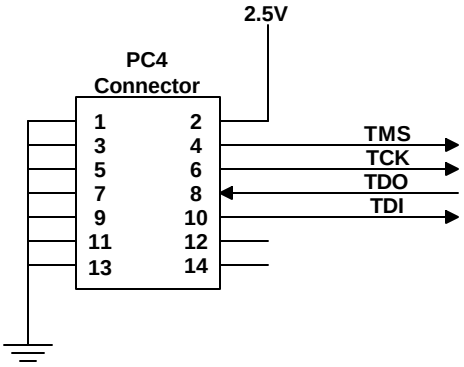


Figure 19 – PC4 JTAG Port Connector

3.12.5 Configuration Modes

The following table shows the Virtex-4 configuration modes.

Table 28 - FPGA Configuration Mode Jumper Settings

Mode	PC Pull-up	Configuration Mode Jumpers			
		1-2 (M2)	3-4 (M1)	5-6 (M0)	7-8 (HSWAP_EN)
Master Serial	Yes	Closed	Closed	Closed	Closed
Master Serial	No	Closed	Closed	Closed	Open
Slave Serial	Yes	Open	Open	Open	Closed
Slave Serial	No	Open	Open	Open	Open
Master SelectMap	Yes	Closed	Open	Open	Closed
Master SelectMap	No	Closed	Open	Open	Open
Slave SelectMap	Yes	Open	Open	Closed	Closed
Slave SelectMap	No	Open	Open	Closed	Open
JTAG	Yes	Open	Closed	Open	Closed
JTAG	No	Open	Closed	Open	Open

3.13 Voltage Regulators

The following figure shows the voltage regulators that are used on Virtex-4 MB development board to provide various on-board voltage sources. As shown in the following figure, a connector is used to provide the main 5.0V voltage to the board. This voltage source is provided to all on-board regulators to generate the 1.2V, 2.5V, and 3.3V voltages.

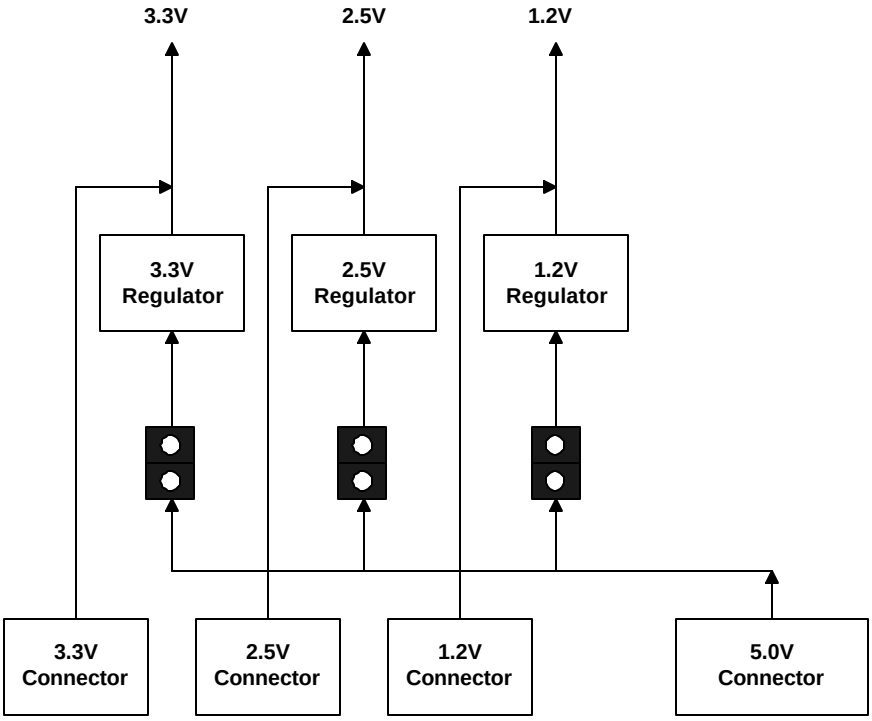


Figure 20 - Voltage Regulators

The following table shows the power provided on the development board for the on-board voltage sources. A 32.5W power adapter (5V @ 6.5A) is used to provide power to the on-board regulators. The following table shows typical power usage on the Virtex-4 MB development board.

Table 29 - Power

Voltage	Current (A)	Power (W)	Comments
1.2V	1.5	1.8	FPGA Core voltage
2.5V	2.0	5.0	FPGA I/O voltage, P240 supply voltage
3.3V	3	9.9	FPGA I/O voltage, P240 supply voltage.
Total Power		**16.7**	

For the on-board digital voltages (1.2V, 2.5V, and 3.3V), if the current provided by the on-board regulator is not sufficient for some applications, the user can directly drive the voltage source and bypass the on-board regulators.

3.14 Bank I/O Voltage

The following table shows the Virtex-4 bank I/O voltages on the Virtex-4 MB development board.

Table 30 – I/O Bank Voltages

Bank #	I/O Voltage
0	2.5V
1	2.5V/3.3V
2	2.5V/3.3V
3	2.5V
4	2.5V
5	2.5V/3.3V
6	2.5V
7	2.5V/3.3V
8	2.5V
9	2.5V
10	3.3V

3.15 P240 Expansion Module Signal Assignments

The following tables show the Virtex-4 pin assignments to the P240 Expansion Module connectors (JX1 & JX2) located on the Virtex-4 MB development board.

Table 31 – P240 Connector Pin Assignments

Virtex-4 FPGA Pin #	I/O Connector Signal Name	JX1 Pin #		I/O Connector Signal Name	Virtex-4 FPGA Pin #
	5.0V	1	2	**5.0V**	
	5.0V	3	4	**5.0V**	
	5.0V	5	6	**5.0V**	
	5.0V	7	8	**5.0V**	
G17	LIO_SE_42	9	10	LIO_SE_43	H26
G18	LIO_SE_40	11	12	LIO_SE_41	H25
C23	LIO_SE_38	13	14	LIO_SE_39	G26
E22	LIO_SE_36	15	16	LIO_SE_37	G25
H23	LIO_SE_34	17	18	LIO_SE_35	F26
H24	LIO_SE_32	19	20	LIO_SE_33	E26
	3.3V	21	22	**3.3V**	
	3.3V	23	24	**3.3V**	
	3.3V	25	26	**3.3V**	

	3.3V	27	28	**3.3V**	
G23	LIO_SE_30	29	30	LIO_SE_31	E25
G24	LIO_SE_28	31	32	LIO_SE_29	D26
F23	LIO_SE_26	33	34	LIO_SE_27	D25
F24	LIO_SE_24	35	36	LIO_SE_25	C26
E23	LIO_SE_22	37	38	LIO_SE_23	C25
E24	LIO_SE_20	39	40	LIO_SE_21	B24
D23	LIO_SE_18	41	42	LIO_SE_19	A24
D24	LIO_SE_16	43	44	LIO_SE_17	B23
	2.5V	45	46	**2.5V**	
	2.5V	47	48	**2.5V**	
	2.5V	49	50	**2.5V**	
	2.5V	51	52	**2.5V**	
C24	LIO_SE_14	53	54	LIO_SE_15	A23
F16	LIO_SE_12	55	56	LIO_SE_13	F11
F15	LIO_SE_10	57	58	LIO_SE_11	C16
F12	LIO_SE_8	59	60	LIO_SE_9	D16
F13	LIO_SE_6	61	62	LIO_SE_7	D15
D13	LIO_SE_4	63	64	LIO_SE_5	D14
C11	LIO_SE_2	65	66	LIO_SE_3	E14
D11	LIO_SE_0	67	68	LIO_SE_1	F14
	GND	69	70	**GND**	
H22	LIO_LVDS_P14	71	72	LIO_LVDS_P15	C21
H21	LIO_LVDS_N14	73	74	LIO_LVDS_N15	B21
	GND	75	76	**GND**	
F20	LIO_LVDS_P12	77	78	LIO_LVDS_P13	F18
E20	LIO_LVDS_N12	79	80	LIO_LVDS_N13	E18
G19	LIO_LVDS_P10	81	82	LIO_LVDS_P11	E21
F19	LIO_LVDS_N10	83	84	LIO_LVDS_N11	D21
	GND	85	86	**GND**	
H20	LIO_LVDS_P8	87	88	LIO_LVDS_P9	D20
G20	LIO_LVDS_N8	89	90	LIO_LVDS_N9	D19
	GND	91	92	**GND**	
D22	LIO_LVDS_P6	93	94	LIO_LVDS_P7	E17
C22	LIO_LVDS_N6	95	96	LIO_LVDS_N7	F17
	GND	97	98	**GND**	
C20	LIO_LVDS_P4	99	100	LIO_LVDS_P5	A22
B20	LIO_LVDS_N4	101	102	LIO_LVDS_N5	A21
	GND	103	104	**GND**	
C19	LIO_LVDS_P2	105	106	LIO_LVDS_P3	A20
D18	LIO_LVDS_N2	107	108	LIO_LVDS_N3	A19
	GND	109	110	**GND**	
C17	LIO_LVDS_P0	111	112	LIO_LVDS_P1	B18
D17	LIO_LVDS_N0	113	114	LIO_LVDS_N1	A18
	GND	115	116	**GND**	
B17	LIO_CLKIN_P	117	118	LIO_CLKIN_1	E13
A17	LIO_CLKIN_N	119	120	LIO_CLKIN_0	D12
	GND	121	122	**GND**	
	GND	123	124	**GND**	
	GND	125	126	**GND**	

	GND	127	128	**GND**	
	GND	129	130	**GND**	
	GND	131	132	**GND**	

Table 32– P240 Connector Pin Assignments

Virtex-4 FPGA Pin #	I/O Connector Signal Name	JX2 Pin #		I/O Connector Signal Name	Virtex-4 FPGA Pin #
	5.0V	1	2	**5.0V**	
	5.0V	3	4	**5.0V**	
	5.0V	5	6	**5.0V**	
	5.0V	7	8	**5.0V**	
W26	RIO_SE_42	9	10	RIO_SE_43	W23
W25	RIO_SE_40	11	12	RIO_SE_41	W24
Y26	RIO_SE_38	13	14	RIO_SE_39	Y23
Y25	RIO_SE_36	15	16	RIO_SE_37	Y24
AA26	RIO_SE_34	17	18	RIO_SE_35	AA23
AB26	RIO_SE_32	19	20	RIO_SE_33	AA24
	3.3V	21	22	**3.3V**	
	3.3V	23	24	**3.3V**	
	3.3V	25	26	**3.3V**	
	3.3V	27	28	**3.3V**	
AB25	RIO_SE_30	29	30	RIO_SE_31	AB23
AC26	RIO_SE_28	31	32	RIO_SE_29	AB24
AC25	RIO_SE_26	33	34	RIO_SE_27	AB21
V20	RIO_SE_24	35	36	RIO_SE_25	W22
AD26	RIO_SE_22	37	38	RIO_SE_23	Y22
W20	RIO_SE_20	39	40	RIO_SE_21	W21
AD25	RIO_SE_18	41	42	RIO_SE_19	AC21
AD19	RIO_SE_16	43	44	RIO_SE_17	AC19
	2.5V	45	46	**2.5V**	
	2.5V	47	48	**2.5V**	
	2.5V	49	50	**2.5V**	
	2.5V	51	52	**2.5V**	
AA16	RIO_SE_14	53	54	RIO_SE_15	AC16
AA15	RIO_SE_12	55	56	RIO_SE_13	AC15
AB14	RIO_SE_10	57	58	RIO_SE_11	AC14
AA14	RIO_SE_8	59	60	RIO_SE_9	AD14
AB13	RIO_SE_6	61	62	RIO_SE_7	AC13
AA13	RIO_SE_4	63	64	RIO_SE_5	AD13
AA12	RIO_SE_2	65	66	RIO_SE_3	AC12
AA11	RIO_SE_0	67	68	RIO_SE_1	AC11
	GND	69	70	**GND**	
Y20	RIO_LVDS_P14	71	72	RIO_LVDS_P15	V21
Y21	RIO_LVDS_N14	73	74	RIO_LVDS_N15	V22
	GND	75	76	**GND**	
AA19	RIO_LVDS_P12	77	78	RIO_LVDS_P13	AC23
AA20	RIO_LVDS_N12	79	80	RIO_LVDS_N13	AC24
AA18	RIO_LVDS_P10	81	82	RIO_LVDS_P11	AC22
Y18	RIO_LVDS_N10	83	84	RIO_LVDS_N11	AB22
	GND	85	86	**GND**	

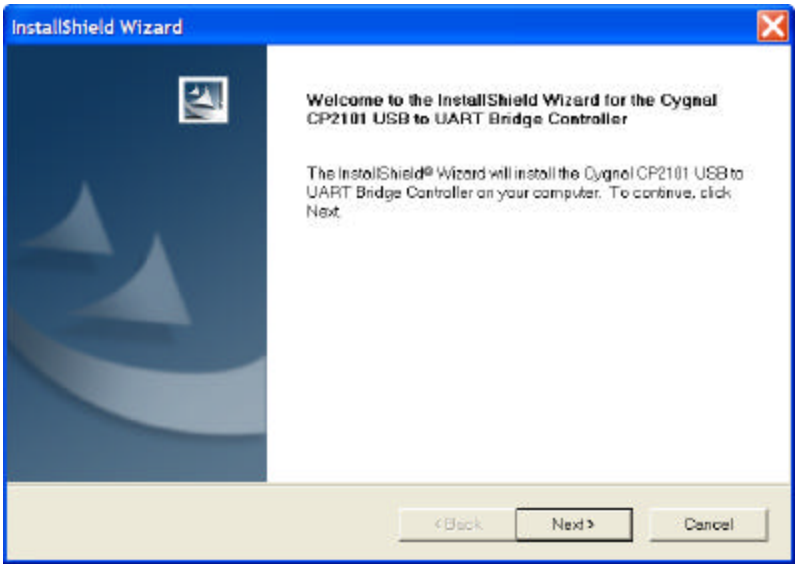
AF24	RIO_LVDS_P8	87	88	RIO_LVDS_P9	AB20
AE24	RIO_LVDS_N8	89	90	RIO_LVDS_N9	AC20
	GND	91	92	**GND**	
AF23	RIO_LVDS_P6	93	94	RIO_LVDS_P7	AD22
AE23	RIO_LVDS_N6	95	96	RIO_LVDS_N7	AD23
	GND	97	98	**GND**	
AF21	RIO_LVDS_P4	99	100	RIO_LVDS_P5	AE21
AF22	RIO_LVDS_N4	101	102	RIO_LVDS_N5	AD21
	GND	103	104	**GND**	
AF19	RIO_LVDS_P2	105	106	RIO_LVDS_P3	AC18
AF20	RIO_LVDS_N2	107	108	RIO_LVDS_N3	AB18
	GND	109	110	**GND**	
AF18	RIO_LVDS_P0	111	112	RIO_LVDS_P1	Y19
AE18	RIO_LVDS_N0	113	114	RIO_LVDS_N1	W19
	GND	115	116	**GND**	
Y17	RIO_CLKOUT_P	117	118	RIO_CLKOUT_1	U7
AA17	RIO_CLKOUT_N	119	120	RIO_CLKOUT_0	U6
	GND	121	122	**GND**	
	GND	123	124	**GND**	
	GND	125	126	**GND**	
	GND	127	128	**GND**	
	GND	129	130	**GND**	
	GND	131	132	**GND**	

4 Revisions

V3.0 Initial release for Rev 3 board Dec 20, 2005

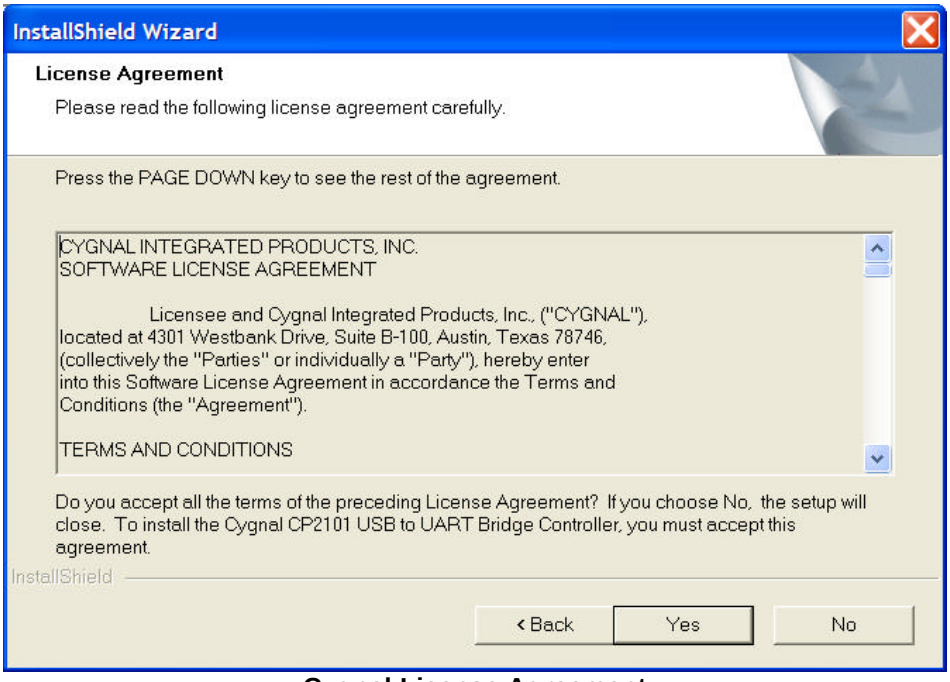
Appendix A

1. Double-click CP2101_Drivers.exe.


InstallShield Wizard
Welcome to the InstallShield Wizard for the Cygnal CP2101 USB to UART Bridge Controller
The InstallShield® Wizard will install the Cygnal CP2101 USB to UART Bridge Controller on your computer. To continue, click Next.
< Back
Next >
Cancel

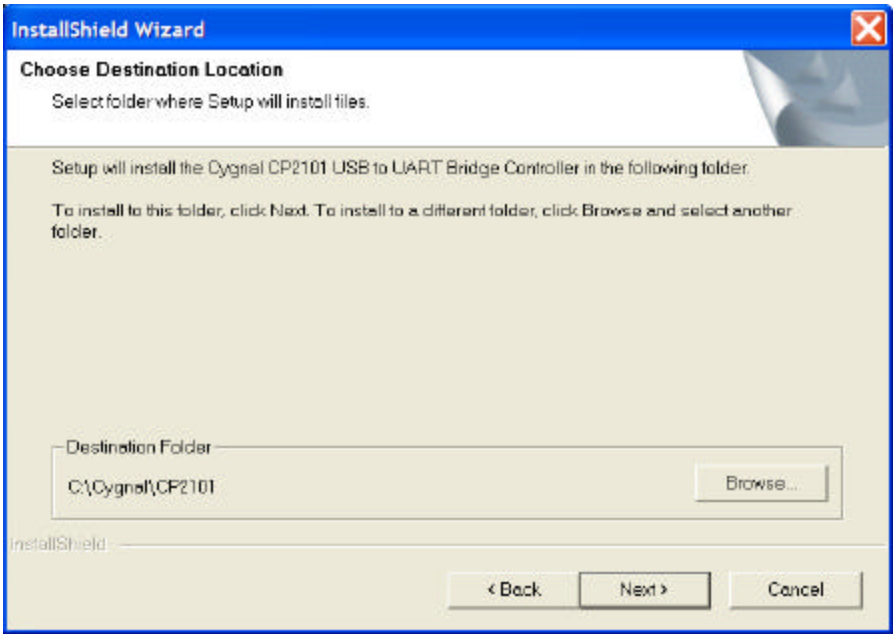
Launching CP2101 Driver Installation

2. Click Next.
3. Read the license agreement and then click Yes.


InstallShield Wizard
License Agreement
Please read the following license agreement carefully.
Press the PAGE DOWN key to see the rest of the agreement.
CYGNAL INTEGRATED PRODUCTS, INC.
SOFTWARE LICENSE AGREEMENT
Licensee and Cygnal Integrated Products, Inc., ("CYGNAL"), located at 4301 Westbank Drive, Suite B-100, Austin, Texas 78746, (collectively the "Parties" or individually a "Party"), hereby enter into this Software License Agreement in accordance the Terms and Conditions (the "Agreement").
TERMS AND CONDITIONS
Do you accept all the terms of the preceding License Agreement? If you choose No, the setup will close. To install the Cygnal CP2101 USB to UART Bridge Controller, you must accept this agreement.
InstallShield
< Back
Yes
No

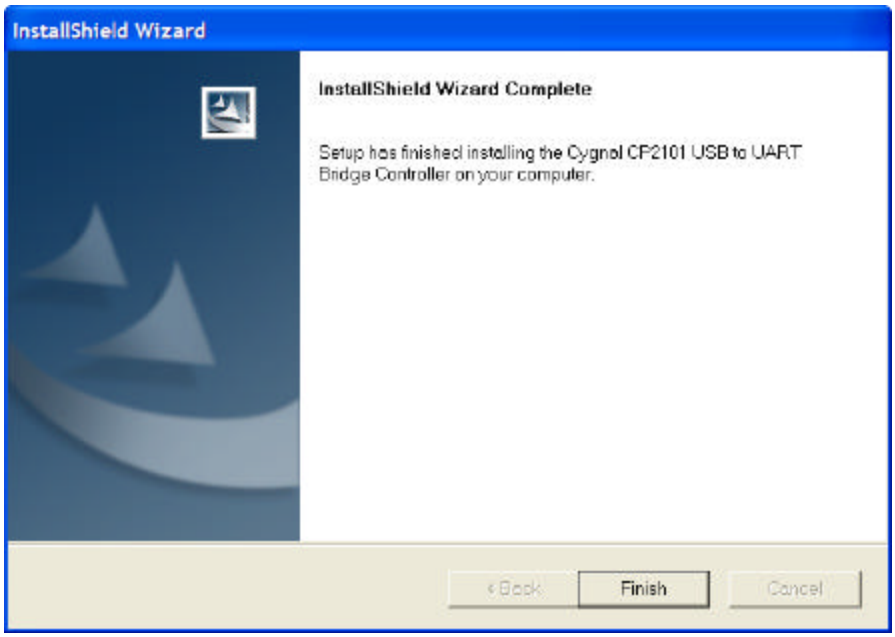
Cygnal License Agreement

4. Browse to an acceptable installation directory, and then click Next.


InstallShield Wizard
Choose Destination Location
Select folder where Setup will install files.
Setup will install the Cygnal CP2101 USB to UART Bridge Controller in the following folder.
To install to this folder, click Next. To install to a different folder, click Browse and select another folder.
Destination Folder
C:\Cygnal\CP2101
Browse...
InstallShield
< Back
Next >
Cancel

CP2101 Destination Location

5. The drivers are extracted to the selected directory. Click Finish once the extraction completes.


InstallShield Wizard
InstallShield Wizard Complete
Setup has finished installing the Cygnal CP2101 USB to UART Bridge Controller on your computer.
< Back
Finish
Cancel

CP2101 Installation Successful

6. To finish the installation, plug the USB cable into the board and a USB port on the PC.

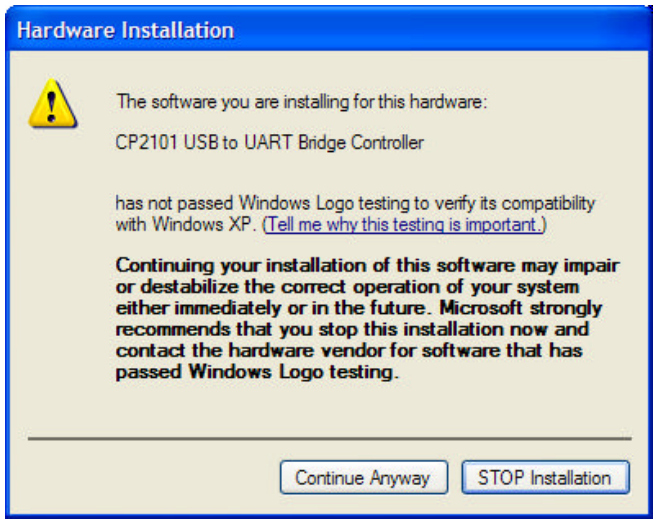
7. Turn the board power switch to the ON position.

8. The **Found New Hardware Wizard** launches. Click the radio button to **Install the software automatically (Recommended)** and then click Next.

Found New Hardware Wizard
Welcome to the Found New Hardware Wizard
This wizard helps you install software for:
CP2101 USB to UART Bridge Controller
If your hardware came with an installation CD or floppy disk, insert it now.
What do you want the wizard to do?
Install the software automatically (Recommended)
Install from a list or specific location (Advanced)
Click Next to continue.
< Back
Next >
Cancel

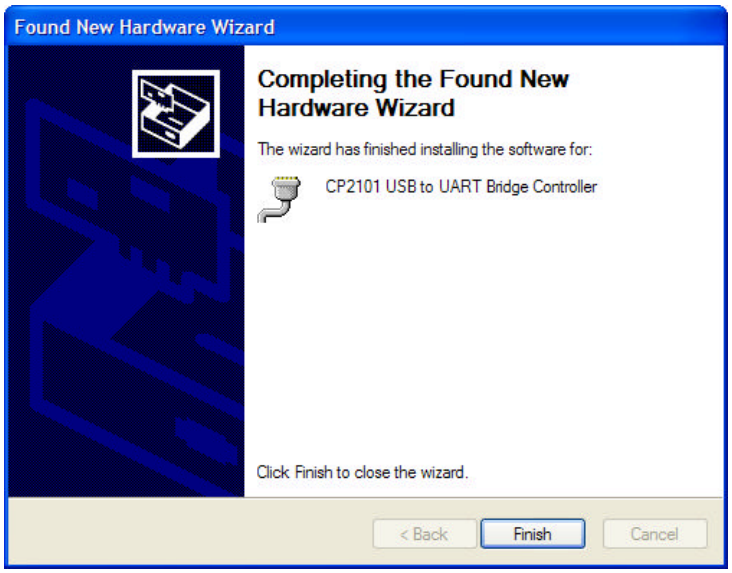
Found New Hardware Wizard

9. The driver installation begins. If installing on WindowsXP, a warning is received stating that Windows Logo testing has not passed, as shown below. Click **Continue Anyway**.


Hardware Installation
The software you are installing for this hardware:
CP2101 USB to UART Bridge Controller
has not passed Windows Logo testing to verify its compatibility with Windows XP. (Tell me why this testing is important.)
Continuing your installation of this software may impair or destabilize the correct operation of your system either immediately or in the future. Microsoft strongly recommends that you stop this installation now and contact the hardware vendor for software that has passed Windows Logo testing.
Continue Anyway
STOP Installation

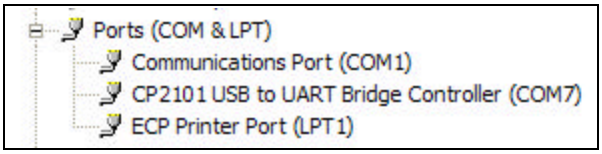
Windows Logo Testing Not Passed

10. The driver installation completes at this point. Click Finish in the **Found New Hardware Wizard**.


Found New Hardware Wizard
Completing the Found New Hardware Wizard
The wizard has finished installing the software for:
CP2101 USB to UART Bridge Controller
Click Finish to close the wizard.
< Back
Finish
Cancel

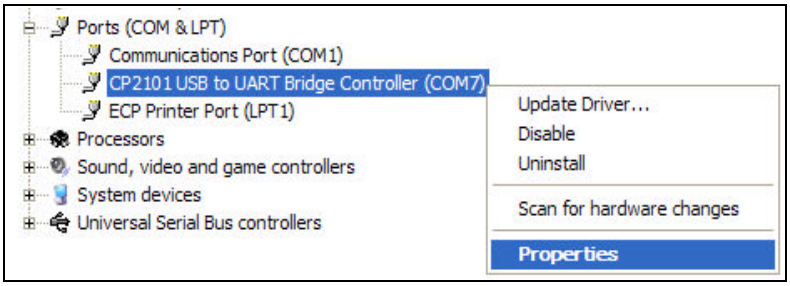
CP2101 Driver Installation Complete

11. Open the Device Manager (Control Panel → System → Hardware tab → Device Manager).
12. Under the **Ports** heading, a new device shows up, called **CP2101 USB to UART Bridge Controller**.



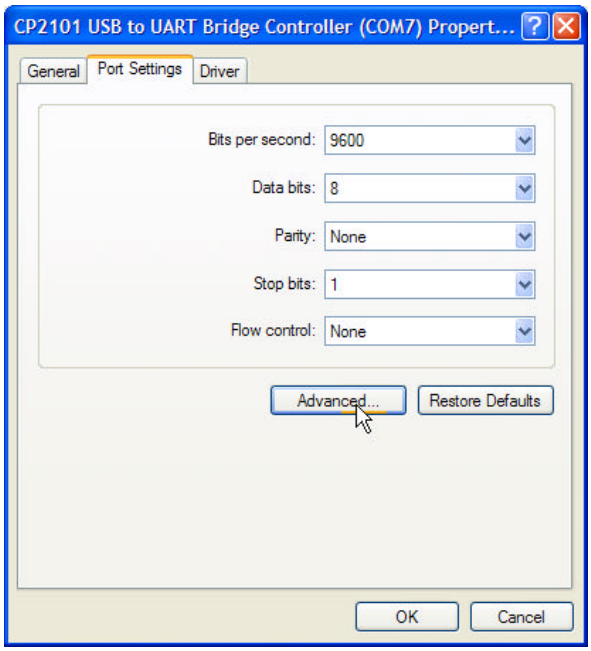
CP2101 Recognized as COM Port

13. If the CP2101 does not show up under ports, it may show up under “Other Devices” with a yellow exclamation mark. In this case, unplug the USB cable, run the setup manually (C:\Cygnal\CP2101\WIN\Setup.exe), and then plug the USB cable back in.
14. The O/S automatically assigns a COM Port number, typically between COM3 and COM7. For consistency, the COM number will be manually changed. Right click on **CP2101 USB to UART Bridge Controller** and select **Properties**.



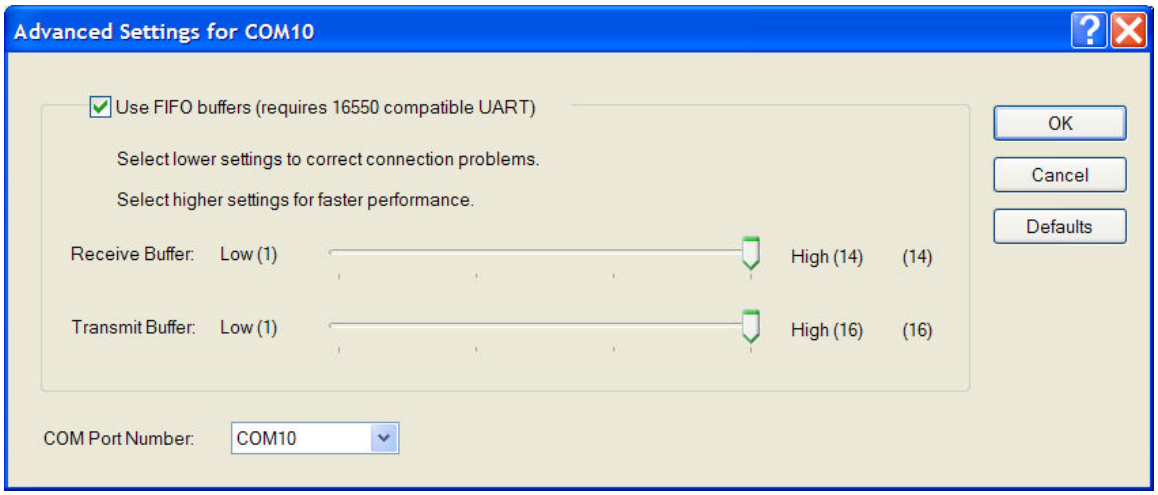
COM Port Properties

15. Change to the **Port Settings** tab and select **Advanced**.



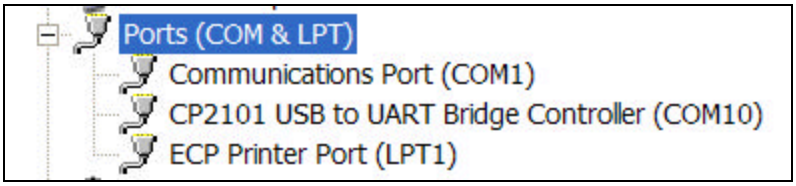
Port Settings – Advanced

16. Select COM10 in the **COM Port Number** field, and then click OK twice.



Changing the COM Port Number

17. Close the Device Manager, and then re-open it. Under **Ports**, the CP2101 USB to UART Bridge Controller is now assigned to COM10, as shown below.



CP2101 Assigned to COM10